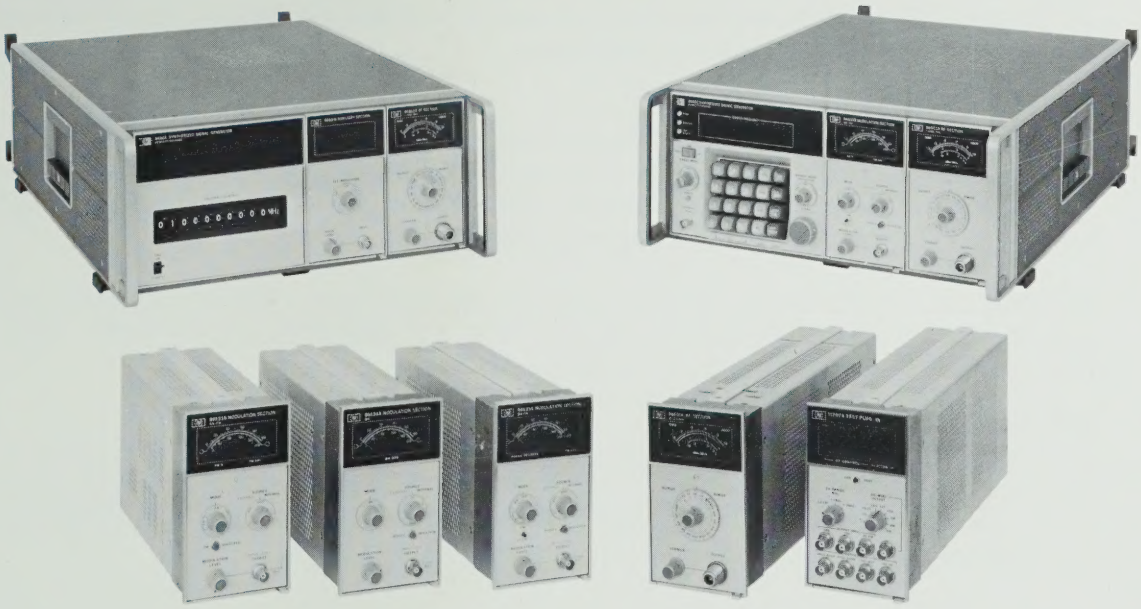
SERVICE MANUAL

8660A
8660B
8660C

SYNTHESIZED SIGNAL GENERATOR SYSTEM



HEWLETT PACKARD

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8660A
8660B
8660C
SYNTHESIZED SIGNAL GENERATOR SYSTEM

EAST 24001 MISSION AVENUE, TAF C-34, SPOKANE, WASHINGTON, U.S.A., 99220

HP Part No. 08660-90070

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HEWLETT PACKARD

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HIGH VOLTAGE

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, if inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

8660A 86631B 86602B

8660C 86632B 86603A

86633B 86634A 86635A

86601A 11707A

Figure 1-1. 8660 Instrument Family

CHAPTER 1
INTRODUCTION

The 8660 instrument family is made up of three mainframes and several modulation and RF plug-ins, as well as a Frequency Extension Module that is used with the high frequency RF plug-ins. The mainframes and plug-ins can be combined to make several different systems. Each of these mainframes and plug-ins has its own Operating and Service Manual that contains information relating to it. This situation may cause confusion when troubleshooting. This manual eliminates the confusion when troubleshooting a system by presenting a uniform method that can be used with any system configuration.

The organization of this manual is as follows:

1. The tests in Chapter 2 are performed to confirm the malfunction.
2. When the malfunction is confirmed, the technician is referred to another chapter of this manual to isolate the problem.
3. When the malfunction is isolated, the technician is referred to one of the Operating and Service Manuals for component-level troubleshooting.

The following equipment is required to test an 8660 system:

Instrument	Model
Oscilloscope	HP 180C/1801A/1820 or the equivalent
Digital Voltmeter	HP 3490
Spectrum Analyzer (86602 or 86603 system) (86601 system)	HP 8555A/8552B/141T HP 8554B/8552B/141T
Microwave Counter (86602 or 86603 system)	HP 5340A
500 MHz Counter (86601 system)	HP 5245L/5253B
Service Kit	HP 11672A
Suggested Equipment:	
Test Plug-In	HP 11707A
Logic Analyzer	HP 1601A

The following instruments and plug-ins are covered in this edition of the manual:

Mainframes	Modulation Sections	RF Sections	Frequency Extension Module
8660A 8660B 8660C	86631A/B 86632A/B 86633A/B 86634A 86635A	86601A 86602A/B 86603A	11661A/B

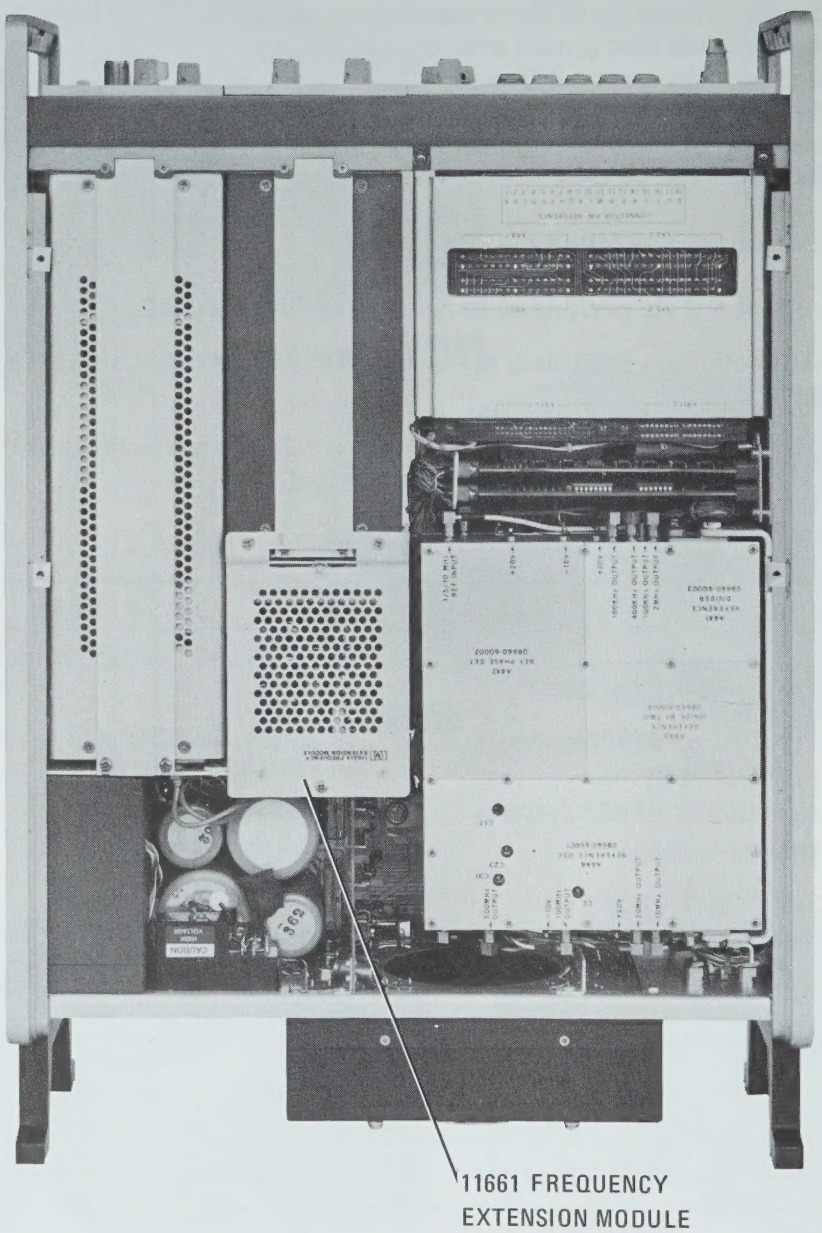


Figure 2-1. Frequency Extension Module Location

CHAPTER 2
PRELIMINARY CHECKS AND OPERATIONAL TESTS

2-1. Check the mainframe line power module (A7) to ensure that it is set for the mains voltage being used and that the fuse is good. (See Figure 2-2). Set reference switch on 8660 rear panel to INTernal.

NOTE

For Option 002 instruments, set switch to EXTernal and apply a 5 or 10 MHz reference sinewave from a crystal oscillator to the rear panel INPUT connector. The reference signal level should be 0.2 Vrms to 2.0 Vrms. (The input impedance of the reference circuitry is 170Ω).

Be sure all plug-ins are securely installed. If an 86602 or 86603 RF Section is installed, remove the mainframe top cover to be sure an 11661 Frequency extension module is installed. (See Figure 2-1.) Set the instrument for local operation by removing any connector that may be plugged into the remote programming input (see Figure 2-2).

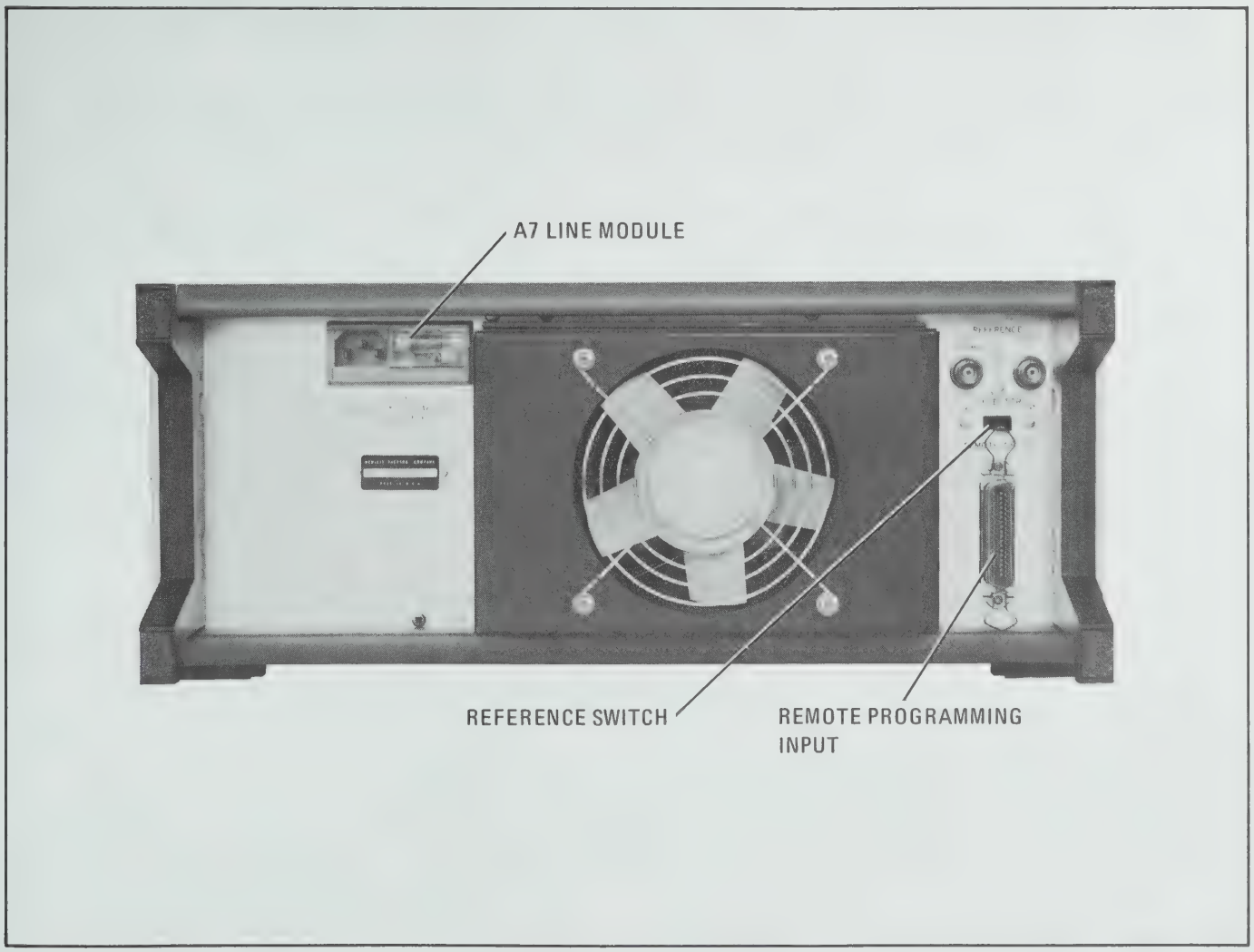


Figure 2-2. 8660 Rear Panel

Set the front panel controls as follows:

Modulation Plug-in	RF Plug-in	8660A
Modulation Mode: OFF Modulation Level: Fully counterclockwise Source: Any position	Output Range: −10 dBm Vernier: Fully clockwise	Frequency control: 1.000000 MHz
Auxiliary Section		**8660B or 8660C**
Ext. Modulation: OFF Pulse Level: Any position		Manual Mode: OFF Sweep Mode: OFF Sweep Rate: Any position

	Test	Result	If Bad Branch To
2-2.	Plug in the instrument and turn the LINE switch ON	Fan starts OVEN indicator on 1.000 000 MHz on readout*	Chapter 3 Step 1 Chapter 3 Step 6** 8660 Mainframe Manual Table 8-5
2-3.	If 8660B or 8660C is being tested perform these tests, if 8660A, skip to Step 2-4 in this chapter. This step tests the operation of the Digital Control Unit (DCU). Later tests will check the interfaces between the DCU and the rest of the instrument.		
2-3a.	Enter a new center frequency within the range of the RF plug-in.	CENTER FREQUENCY displays entered frequency exactly.	Table 8-6, 8660B Manual. Table 8-10, 8660C Manual.
2-3b.	Enter a center frequency in Hz below 10 kHz.	As in 2-3a. OUT OF RNG indication comes on.	Table 8-8 in 8660B Manual Table 8-12 in 8660C Manual Table 8-22 in 8660B Manual Table 8-26 in 8660C Manual
2-3c.	Enter arbitrary center frequencies using kHz, MHz and GHz units within the RF plug-in range.	Readout properly positioned and appropriate unit's lamp lit.	Tables 8-10 and 8-11 in in 8660B Manual. Tables 8-14 and 8-15 in in 8660C Manual
2-3d.	Enter STEP ↑ amount within RF range and then STEP ↓ to original frequency.	CENTER FREQUENCY displays new frequency after STEP ↑ and original frequency after STEP ↓.	Tables 8-12 and 8-13 in 8660B Manual Tables 8-16 and 8-17 in 8660C Manual.

*8660A will have a readout only if option 009 is installed. If an 8660B or 8660C displays only one or two partial digits, go to Table 8-9 in the 8660B or 8660C Operating and Service Manuals. If display is dim, check +4V supply.

**The OVEN light may not come on if the instrument has been connected to the power line for several minutes. The OVEN light will extinguish in approximately 10-15 minutes indicating the crystal oscillator oven is up to temperature. The oven is powered whenever line power is connected to the instrument regardless of power switch setting.

	Test	Result	If Bad Branch To
2-3e.	Switch MANUAL MODE to STEP. Turn MANUAL SWEEP clockwise and counterclockwise.	CENTER FREQUENCY should increase in step equal to previously entered STEP size. Frequency decreases in steps equal to step size.	Table 8-14 in 8660B Manual. Table 8-18 in 8660C Manual.
2-3f.	Switch MANUAL MODE successively through FINE, MEDIUM and COARSE, and tune the MANUAL SWEEP knob clockwise and counterclockwise.	Frequency displayed increases and decreases in steps of FINE: 1 Hz MED: 1 kHz COARSE: 1 MHz	Tables 8-15, 8-16 and 8-17 in 8660B Manual. Tables 8-19, 8-20 and 8-21 in 8660C Manual.
2-3g.	Check AUTO; SINGLE; and then MANUAL positions on SWEEP MODE control. Set to AUTO and SLO. In SLO mode Out of Range Lamp should flash 5 seconds on — 5 seconds off. (8660C will spend 25 seconds on — 25 seconds off). 86601A: 10 kHz center frequency 10 kHz sweep width 86602 or 86603 1 MHz center frequency 1 MHz sweep width.		In 8660B Manual, Table 8-19 for auto sweep, Table 8-20 for single sweep, Table 8-21 for manual sweep. In 8660C Manual, Table 8-23 for auto sweep, Table 8-24 for single sweep, Table 8-25 for manual sweep.
2-3h.	Check sweep ramp OUTPUT (0-8V) on oscilloscope (or voltmeter using SLO sweep rate).	Voltage starts at 4V, rises to 8V, drips to 0V and sweeps 0 to 8V until sweep is turned off.	Service Sheet 33 in 8660B and 8660C Manuals.
2-3i.	Check operation of KYBD, STEP ↓↑ and SWP WIDTH display pushbuttons.	CENTER FREQUENCY displays the data entered into the register corresponding to the pushbutton. If no data has been entered will show zero or blank.	Tables 8-23, 8-24 or 8-25 in 8660B Manual. Tables 8-27, 8-28, or 8-29 in 8660C Manual.
2-4.	Check RF output level by adjusting the spectrum analyzer for +10 dBm log reference level with 40 dB of input attenuation set on its RF section. Connect the system RF Section Output to the Analyzer input. RF section VERNIER: 0 dB on its meter. OUTPUT RANGE: 1 V. CENTER FREQUENCY: any frequency below 1300 MHz within the range of the RF Section that the spectrum analyzer can easily display. The output signal trace should reach the top graticule line on the spectrum analyzer display. If it does not, refer to Chapter 4 in this manual.		
2-4a.	Set the OUTPUT RANGE control down in 10 dB increments. By switching each step to —80 dBm, all attenuator sections will be checked.	The displayed signal drops in 10 dB increments.	Chapter 4

	Test	Result	If Bad Branch To
2-4b.	With the OUTPUT RANGE set at any level, vary the VERNIER control setting.	Spectrum Analyzer display tracks RF section meter reading over a 13 dB range.	Chapter 4
2-5.	Set the OUTPUT RANGE to 0 dBm, connect the digital counter input to the system RF output and connect the system rear panel REFERENCE OUTPUT to the counter 10 MHz REFERENCE INPUT. These tests can also be performed with the 8660 locked to the counter time base (5 or 10 MHz) although noise performance will likely be degraded. In this step we will test functioning all of the phase lock loops and thereby test the interface between the DCU, the mainframe, and Frequency Extension Module, if one is installed. If an 8660A is being tested, turn the thumb switch(es) to correspond to the STEP ↑ increment.		
2-5a.	Enter 11.111 111 MHz Center Frequency.	11.111 111 MHz ± 1 Hz on on counter.	Chapter 5
	Step the frequency in 11.111 111 MHz steps to 99.999 999 MHz.	22.222 222 MHz ± 1 Hz to 99.999 999 MHz ± 1 Hz	Chapter 5
2-5b.	Enter 109.999 999 MHz Center Frequency.	109.999 999 MHz ± 1 Hz on counter.	Chapter 5
2-5c.	For High Frequency RF Sections only, enter 111.111 111 MHz Center Frequency.	111.111 111 MHz ± 1 Hz on counter.	Chapter 5
2-5d.	Enter 1299.999 999 MHz Center Frequency.	1299.999 999 MHz ±1 Hz on counter.	Chapter 5
2-5e.	Enter 1300 MHz Center Frequency.		
2-5f.	Enter 1 Hz STEP ↑.	The indicated output frequency should not change.	
2-5g.	STEP ↑ once more.	1300.000 002 MHz ± 1 Hz on counter.	
2-5h.	Enter 2599.999 998 MHz Center Frequency.		
2-5i.	STEP ↑1 Hz.	Output frequency should not change.	
2-5j.	STEP ↑ 1 Hz.	Out of Range Light should flash once and frequency should not change.	
2-6.	This step will check the modulation signals generated by the 86632, 86633 and 86635 Modulation Sections.		

Test		Result	If Bad Branch To
2-6a.	Enter 10 MHz center frequency at 0 dBm (arbitrarily chosen). Set Modulation Section: Source: 400 Internal Modulation Level: 50% as indicated on meter.	Connect spectrum analyzer to RF output connector. The first sideband pair should be 12 dB down 400 Hz from the carrier.	Chapter 8 Step 1.
2-6b.	Switch Modulation Source: 1000 internal 50% modulation	Sidebands 12 dB down 1 kHz from carrier.	Chapter 8 Step 6.
2-6c.	Set mode switch to FMx0.1. Source remains at 1000 INTERNAL. Turn the modulation level control fully counterclockwise, then slowly clockwise until the first carrier null is reached.	The modulation meter should indicate 2.4 kHz ± 500 Hz deviation (19 to 29 on the meter).	Continue to 2-6d.
2-6d.	Continue clockwise until the second null is reached.	5.5 kHz ± 500 Hz deviation (50 to 60 on the meter).	Continue to 2-6e.
2-6e.	Switch to FMx1 and turn the modulation level control fully clockwise.	See Figure 2-3	Continue to 2-6f.
2-6f.	Switch to FMx10 (86632 or 86635).	See Figure 2-4.	If 2-6c, 2-6d, or 2-6e bad, Chapter 9.
2-6g.	Press the FM CF CAL button (86632 or 86635).	Modulation drops to zero for about 5 seconds. CF is phase locked during calibration cycle.	Chapter 10.
2-6h.	If an external 1000 Hz modulation source is available, connect it to input/output connector at level of 1.0 to 2.0 Vrms. Set Source to: AC EXTERNAL. Repeat 2-6a through 2-6g. Set source to DC EXTERNAL and repeat 2-6a thru 2-6g. Set modulation level: clockwise. Adjust external signal for full scale reading on modulation meter. This typically requires 1.8 to 2.0 Vrms. Repeat 2-6a thru 2-6f.		Chapter 10.

Test	Result	If Bad Branch To

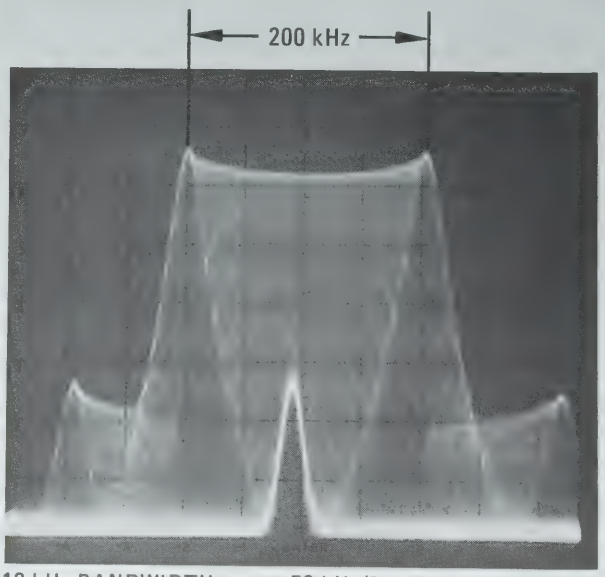


Figure 2-3. FM x 1 Display

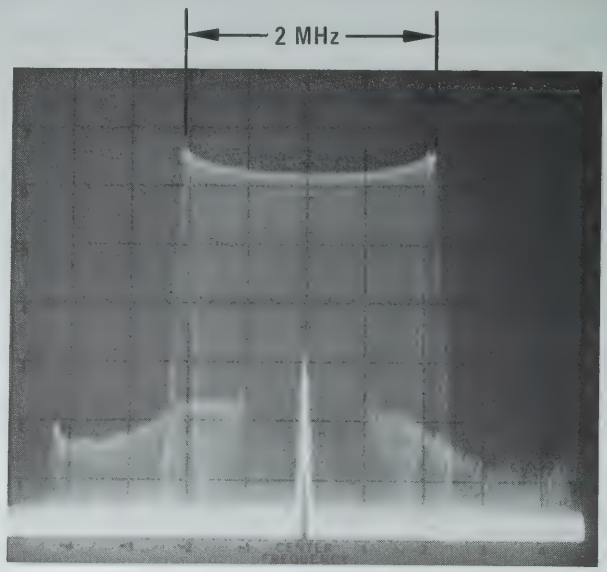


Figure 2-4. FM x 10 Display

2-7.	This step applies only to instruments equipped with phase modulation circuitry (86634 or 86635 with an 86603 Option 002). Set center frequency below 1300 MHz.		
2-7a.	Set ϕM MODE on modulation section. Set SOURCE to 1000 Hz. Turn LEVEL control fully counterclockwise, and then clockwise until the first sidebands and carrier are of equal level on the spectrum analyzer display. The modulation meter should indicate 82° ± 5° (±5% of full scale).		Chapter 11
2-7b.	Set center frequency above 1300 MHz. The modulation level should remain at 82° but the meter scale should change to the 0 to 200° range.		Chapter 11
2-7c.	Set SOURCE to 400 Hz. The sideband amplitudes should not change; they should merely move closer to the carrier.		Chapter 11
2-7d.	Set modulation level to 200° indicated on meter. The spectrum analyzer display should be similar to Figure 2-5.		Chapter 11

	Test	Result	If Bad Branch To

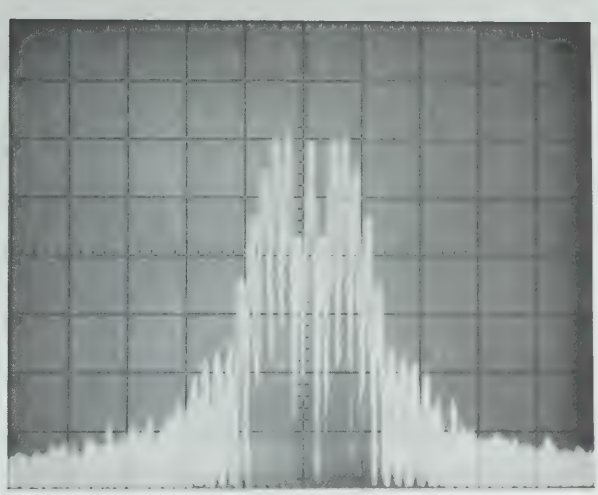


Figure 2-5. Phase Modulation

2-8.	All functions have now been checked for proper operation in local mode. To test the instrument in remote mode, refer to the 8660 Operating and Service Manual. Section III for remote programming instructions. Prepare a program or card-set compatible with your remote programming device to repeat the tests run in local mode. The phase lock loops tests may be deleted if desired and a simplified test to check programming at the frequency extremes of the RF Section may be substituted.		Table 8-26 of the 8660B Manual or Figure 8-49 of the 8660A Manual or Table 8-30 of the 8660C Manual.

CHAPTER 3
MISCELLANEOUS TURN-ON PROBLEMS

Fan does not turn on.

3-1. Unplug the instrument - recheck the main line fuse (A7F1).

3-2. Remove the mainframe bottom cover.

3-3. Locate the A20 rectifier board and find tie point $\overset{SW}{9}$ (see Figure 3-1).

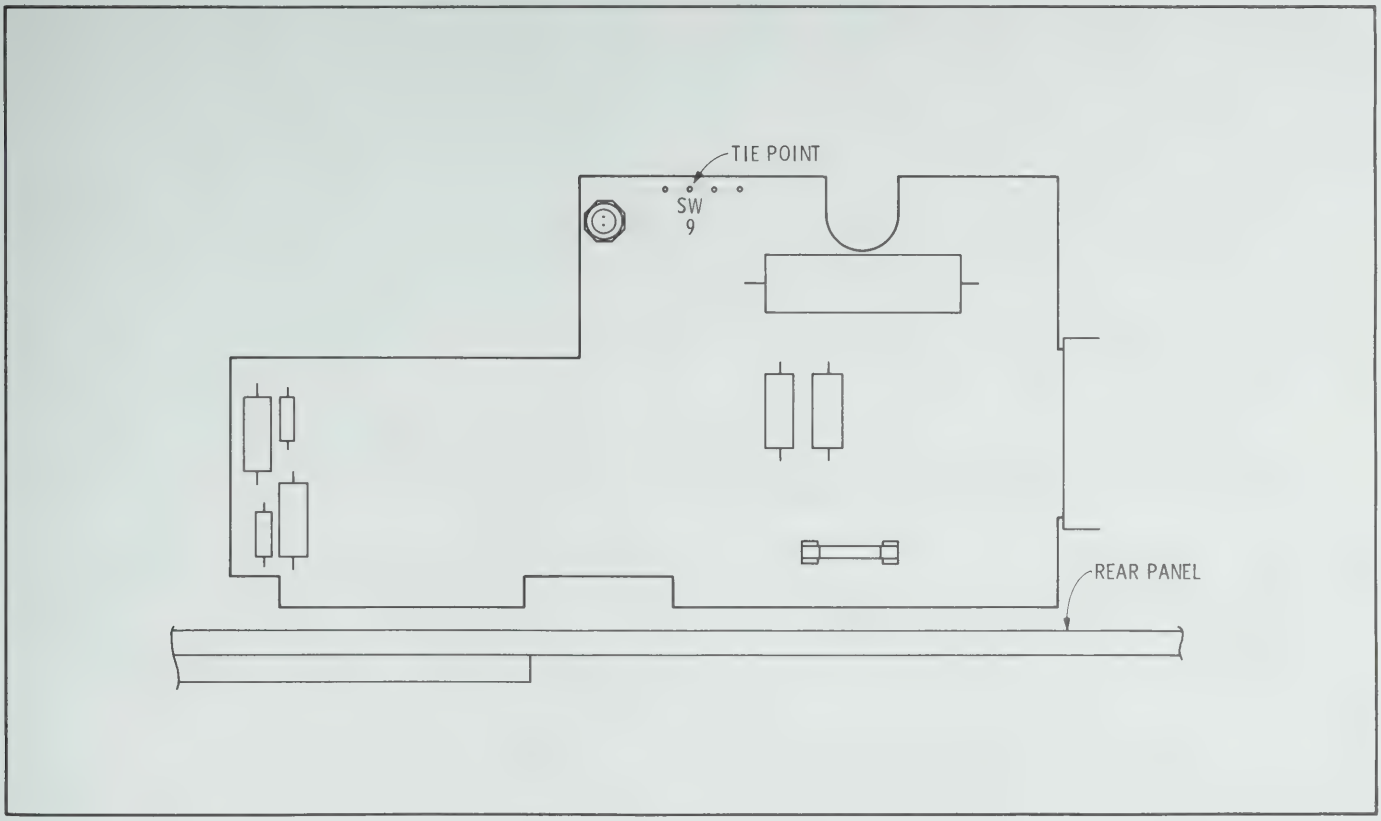


Figure 3-1. A20 Rectifier Board

3-4. With the instrument unplugged, measure the resistance to ground at tie point $\overset{SW}{9}$ see Table 3-1.

Table 3-1. $\overset{SW}{9}$ *ON-OFF Conditions*

Line Switch Position	Reading
ON	0Ω
STBY	Charging Capacitor Ultimate value ≈10 kΩ

If both switch positions are OK, continue to Step 3-5. If ON reading is high, A1S1 or interconnecting wiring is likely defective. If OFF reading is bad, go to Section VIII of the Mainframe Operating Service Manual to troubleshoot the power supply.

3-5. Check the voltage applied to the fan motor (should be ≈115 Vac). If the voltage is proper, check the fan. If the voltage is improper, check relay A20K1 then go to Section VIII of the Mainframe Operating and Service Manual to troubleshoot the power supply.

OVEN light does not come on when instrument is first turned on.

3-6. Turn off and *unplug* instrument for 10 minutes.

3-7. Remove mainframe top cover. Locate the following test points in Table 3-2.

Table 3-2. OVEN Line Test Point Locations

Instrument	Test Point
8660A	A3XA1 pin 12 (bottom pin) of A3A1 Front Interface Board
8660B 8660C	OVN test point on DCU Mother Board

Measure the resistance from the test point to ground. It should be zero ohms.

If OK, continue to 3-8.

If ≈50Ω, the lamp is good and A21, interface board or interconnecting wiring is defective. Go to the Mainframe Manual Section VIII for schematics to isolate the defect.

3-8. Plug in and turn on instrument. Does OVEN lamp come on? If yes, wait 10-15 minutes to see if it will extinguish normally. (If not, replace A21 or find short in wiring). If no, measure the voltage at the same test points, previously located.

Table 3-3. OVEN Line Resistance

OVEN Condition	Voltage	Resistance (OFF)
Cold	0V	0Ω
Hot	5V	40-80Ω

If the readings are not proper, remove the Front Interface Board (A3A1) to isolate the lamp from the A21 assembly. Go to the Mainframe Manual Section VIII to continue troubleshooting from the Front Interface Board Schematic.

CHAPTER 4
RF POWER OUTPUT PROBLEMS

Several types of RF output power problems are covered in this chapter. Select from the following list, the problem description that best describes your problem. Begin troubleshooting at the paragraph number indicated.

1. No power output. Go to paragraph 4-1.
2. None of the 10 dB steps work. Go to paragraph 4-5.
3. At least one of the 10 dB steps works (but not all). Go to paragraph 4-10.
4. The Vernier does not work. Go to paragraph 4-12.
5. Power output low. Go to paragraph 4-13.
6. Power output low above 1300 MHz. Go to paragraph 4-15.

4-1. There are four basic causes of no apparent output power (assuming you have reached this point by following the procedure in this manual).

a. A defective phase lock loop in the mainframe or frequency extension module. Continue with Step 4-2.

b. A defective amplifier in the RF plug-in. Continue with 4-2.

c. Output attenuator at maximum attenuation. Go to paragraph 4-9.

d. The "A" register or output register bad (DCU). Continue with 4-2.

4-2. To check the phase lock loops, replace the RF section with Test Plug-In 11707A. Measure the levels and frequencies shown in the following tables. If an 11707A is not available, use one of the alternate test locations shown in the table.

Table 4-1. Phase Lock Loop Outputs and Test Points

Frequency	Power at 11707A	J6 Pin Number*	Power at J6	Internal Test Point
500 MHz	>0 dBm	61	>+3 dBm	A4J9
100 MHz	>+7 dBm	65	>+10 dBm	A4J8
20 MHz	>+3 dBm	62	>−6 dBm	A4J7
350-450 MHz	>+6 dBm	64	>+10 dBm	A4J12
20-30 MHz	>−11 dBm	63	>−7 dBm	A2 Jack Labeled SL1
2.75-3.95 GHz	>+7 dBm	Mainframe P3	>+10 dBm	J2 on 11661A
3.95-4.05 GHz	>−6 dBm	Mainframe P5	>−4 dBm	J1 on 11661A

*These pins are coaxial; do not attempt to measure the signal at these pins if you do not have the appropriate adapter; HP Part Number 11672-60008. Otherwise the pins may be permanently damaged.

4-3. If any phase lock loop is bad, branch to Chapter 5 of this manual for more troubleshooting. If all of the phase lock loop outputs are OK, check the +20V ±100 mV and —10V ±50 mV supplies at the front of the 11707A or at pins 11 and 12 of J6. The microcircuit output amplifier uses these voltages. (Since it is easy to do, check the presence of all power supply voltages while the digital voltmeter is connected to the 11707A.)

4-4. If all the power supplies are OK, extend the RF section with its covers removed on cable 11672-60001. (If a high frequency plug-in is being tested, cables 11672-60002 and 11672-60006 must also be used).

Measure the input signal to the output amplifier or preamplifier as in Table 4-2.

Table 4-2. RF Preamplifier Inputs

RF Section	Test Input To Assembly Number	Level	Frequency
86601A	A6	—30 dBm	0.01—110 MHz
86602 & 86603	A6	—25 dBm to —85 dBm	1 — 1300 MHz

If the signal is correct, go to Section VIII of the RF Section Operating and Service Manual to troubleshoot the final output components and the Local/Remote interface. If the signal is not correct, the problem is localized to the RF seciton input circuitry and mixers; go to Section VIII of the RF Section Manual.

4-5. *None of the 10 dB attenuation sections switch but there is RF power out.* Check the ±21 volt unregulated power supplies and the +5.25V regulated power supply in the mainframe on A20 and A5. If any of them are bad, check the fuse for that supply then go to Section VIII of the Mainframe Operating and Service Manual to repair the power supply

4-6. If the supplies are good, turn off instrument, install the RF section, with its cover removed, on an 11672-60001 extender cable. Turn on instrument. Check the LCL/RMT line at pin E of the edge connector J on the Logic and Driver circuit board (A11XA10 in 86601, A12XA11 in 86602, and 86603). *This line should be logic high (>+2.4V) for local operation.* If LCL/RMT is low (<+0.8V) refer to the Mainframe Manual to trace the LCL/RMT line in the DCU and interface boards. Otherwise continue.

4-7. Check the voltages at the RF Section output attenuator switching pins (See Appendix 3 for location). The voltages should be typically +21V or —21V depending on the attenuation value selected. See Table 4-2.

It would be unusual, but if the voltages all switch properly and the attenuation does not change, the output attenuator is defective.

4-8. If none of the RF Output attenuator pins switch properly, the local/remote multiplexer (selector) on the Logic and Driver board (A10 in 86601, A11 in 86602 and 86603) is the most probable cause, although there could be an open trace on the RF Section mother board or a defective Attenuator Driver circuit board (A9).

Table 4-3. Attenuation Switching Voltages

dB / dBm	86601				86602 and 86603*			
	10	20	40	80 (40-40)	10	20	40	80 (40-40)
+ 10	-21	-21	-21	-21	-21	-21	-21	-21
0	+21	-21	-21	-21	-21	-21	-21	-21
- 10	-21	+21	-21	-21	+21	-21	-21	-21
- 20	+21	+21	-21	-21	-21	+21	-21	-21
- 30	-21	-21	+21	-21	+21	+21	-21	-21
- 40	+21	-21	+21	-21	-21	-21	+21	-21
- 50	-21	+21	+21	-21	+21	-21	+21	-21
- 60	+21	+21	+21	-21	-21	+21	+21	-21
- 70	-21	-21	-21	+21	+21	+21	+21	-21
- 80	+21	-21	-21	+21	-21	-21	-21	+21
- 90	-21	+21	-21	+21	+21	-21	-21	+21
-100	+21	+21	-21	+21	-21	+21	-21	+21
-110	-21	-21	+21	+21	+21	+21	-21	+21
-120	+21	-21	+21	+21	-21	-21	+21	+21
-130	-21	+21	+21	+21	+21	-21	+21	+21
-140	+21	+21	+21	+21	-21	+21	+21	+21

*86603 goes to —130 dBm range.

4-9. *RF Section Output Attenuator (A13 Assembly) stuck at maximum attenuation.* Check LCL/RMT and PWR DET lines on the Logic and Driver board (A10 in 86601, A11 in 86602 and 86603). If the instrument is programmed to be in remote, the attenuation is automatically programmed to —140 dB at turn on for RF sections with prefix 1335A or higher.

4-10. Turn off instrument; extend the RF Section with its cover removed on cable 11672-60001. Turn instrument ON. Measure the voltages at the switching pins (10D, 20D, 40D and 80D lines) on the RF output attenuator (A13 or at the Mother board connector left rear). If all are OK (as indicated in Table 4-3), replace the attenuator.

If not OK, turn instrument OFF, install the Attenuator Driver board (A8 in 86601, A9 in 86602 and 86603) on an extender board. Turn instrument on. Check the attenuation data into the extended board at the edge connector.

Pin M	10 dB data
Pin L	20 dB data
Pin K	40 dB data
Pin J	80 dB data

ON = >2.4V OFF = <0.8V

4-11. If data is OK, repair the extended board.

If data not OK, remove the board from the extender and recheck the data. If data is OK with board removed, repair the board removed.

If data is still bad with board removed, repair the Logic and Driver board (A10 in 86601A, A11 in 86602 and 86603), the A1S1 switch assembly or interconnecting wiring.

4-12. *RF output vernier does not work.* Turn off instrument. Extend RF section with cover removed on cable 11672-60001. Install Reference Assembly (A9 in 86601, A10 in 86602 and 86603) on extender board. Turn on instrument. Measure the voltage at pin 10 of the edge connector on the extended board. Turn the Vernier clockwise. The voltage at pin 10 should be —1V and should approach zero as the vernier is turned clockwise. If OK, repair the Feedback Amplifier board or the Modulator Assembly. If not OK, repair the Reference Assembly or replace the Vernier as required.

4-13. *Power output low.* Turn off instrument. Extend with the cover removed on cable 11672-60004. Remove the input connector to the RF output amplifier in 86602 and 86603, or the RF amplifier in the 86601. Turn on instrument. Measure the power from the input cable on a spectrum analyzer. See Table 4-2 for levels and frequencies. If not OK, go to the RF Section Manual , Section VIII, to repair the input mixing circuitry. If OK, continue with 4-14.

4-14. Reconnect the input connector and disconnect the output connector from the output amplifier (not the preamp). Connect spectrum analyzer to amplifier output and turn vernier fully clockwise.

86601	+13 dBm ± 0.5 dBm
86602	+10 dBm ± 0.5 dBm
86603	+10 dBm ± 0.5 dBm

If OK, check output attenuator and replace if defective. If power not OK, perform the RF Output adjustment procedures in Section V of the RF Section Operating and Service Manual. If OK, return to Chapter 2 of this manual to continue at Step 2-4.

If still not OK, repair the ALC circuitry at the completion of the adjustments or replace the RF output amplifier or preamplifier as required.

4-15. Power output low above 1300 MHz. Check the output of the A20, doubler power supply. It should be +24V ±0.1V or +22V ±0.1V depending on the type of doubler installed. Check the ALC BW control signal which goes to the A4 and A3 assemblies. This signal should be high for frequencies 1300 MHz and above. Also check the output of the A21 filter drive assembly. If these signals are correct, the problem is in the A22 doubler assembly and this unit should be replaced by a rebuilt exchange assembly.

CHAPTER 5
RF OUTPUT FREQUENCY INCORRECT OR UNLOCKED

There are two basic failure catagories that will lead you to this section. (1) the output signal is unlocked or (2) the output is locked at a wrong frequency (i.e., the output center frequency differs from the programmed center frequency).

5-1. Remove the RF section and install Test Plug-in 11707.

Check fixed frequency reference signals with a frequency counter and power meter. Be sure the counter is still referenced to the 8660 timebase. Refer to Table 4-1 for test points if the test plug-in is not available.

	without 11707A	with 11707A
500.000 000	>+3 dBm	>0 dBm
100.000 000	>+10 dBm	>+7 dBm
20.000 000*	>−6 dBm	>+3 dBm**

*Precise if 86632 or 86635 are not in FM Mode.
**This signal is amplified in the 11707.

If all are correct, skip to paragraph 5-5.

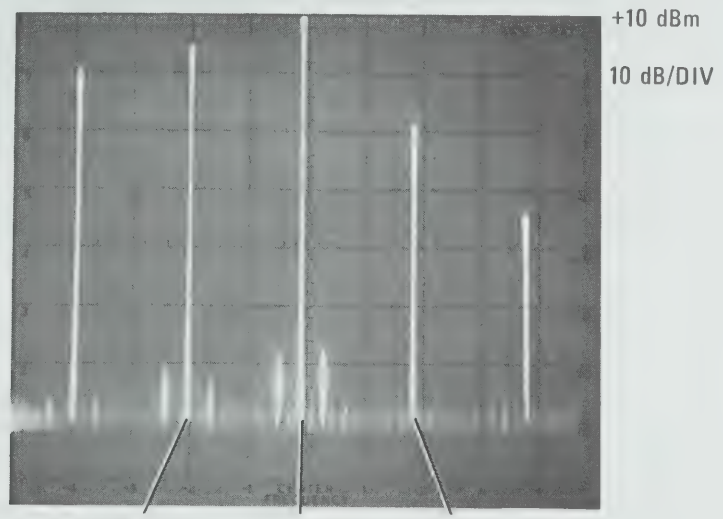


Figure 5-1. 500 MHz Reference Signal

5-2. If any of the above are incorrect, remove the mainframe top cover and repeat the measurements directly on the A4 assembly to check for possible wiring and connection problems.

5-3. If still bad, measure the reference output signal at the rear panel OUTPUT connector. The signal should be 10 MHz at 0.5 to 1 Vrms when connected to a 170Ω load.

5-4. If the reference output is defective, refer to the mainframe Operating and Service Manual, Section VII, for aid in troubleshooting assemblies A21 and A22. If the reference output is OK, refer to the mainframe Operating and Service Manual, Sections VIII and V for aid in troubleshooting and adjusting the Reference Section Assembly A4.

5-5. Measure the output frequency and power of two of the mainframe tunable phase lock loops as follows. See Appendix A, Tables 1 and 6 in this manual, for center frequency vs. loop frequency information.

Table 5-1. Mainframe Loop Outputs

Frequency Range	Loop Name	Power
20.000 001 to 30.000 000 MHz *350—450 MHz	SL1 High Frequency	> −11 < − 3 dBm > +6 < +15 dBm
*360—450 MHz if an 86602 or 86603 is installed.		

If both loops are OK and an 86602 or 86603 is involved, branch to Chapter 6 of this manual to check the Frequency Extension Module, Model 11661.

5-6. *If the High Frequency Loop is malfunctioning*, check the power and frequency of the 10 MHz reference signal on A4A3 output. It should be >−15 dBm on a spectrum analyzer. If OK, then check the digital frequency data feeding A4A6. The data is positive (high= on) in a BCD format. If OK, refer to the Mainframe Operating and Service Manual, Section VIII , to troubleshoot A4A3. If the signal from A4A3 is defective, refer to the Mainframe Manual, Section VIII, for aid in its repair. If the digital information is incorrect, unsolder the suspected leads at the outside of the A4 housing feedthrough and remeasure the levels. If data is correct with the leads unsoldered, A4A3 or the feedthrough needs repair. If data is still defective, the problem is in the DCU (probably A10A10 in 8660B and 8660C or A1A8 in 8660A) or in the interface boards or wiring. Refer to the DCU troubleshooting information in the Mainframe Manual, Section VIII.

5-7. *If the SL1 output is malfunctioning*, considerable insight into the location of the failure may be gained by noting which digits of the output frequency are incorrect. Four phase lock loops are involved in feeding signals to Sum Loop 1. The following table lists the digits controlled by each of the four loops. (Digit 1 is defined here as the digit which controls one hertz steps; the least significant digit). See Table 5-2 and Figure 5-2. Continue to paragraph 5-8 for troubleshooting.

Table 5-2. Digits Controlled by Mainframe Loops

Digit / Loop	MHz D7	100's of kHz D6	10's of kHz D5	kHz D4	100's of Hz D3	10's of Hz D2	Hz D1
N1	←	←					
N2			←	←	←		
N3						←	←
SL1	←	←	←	←	←	←	←
SL2			←	←	←	←	←

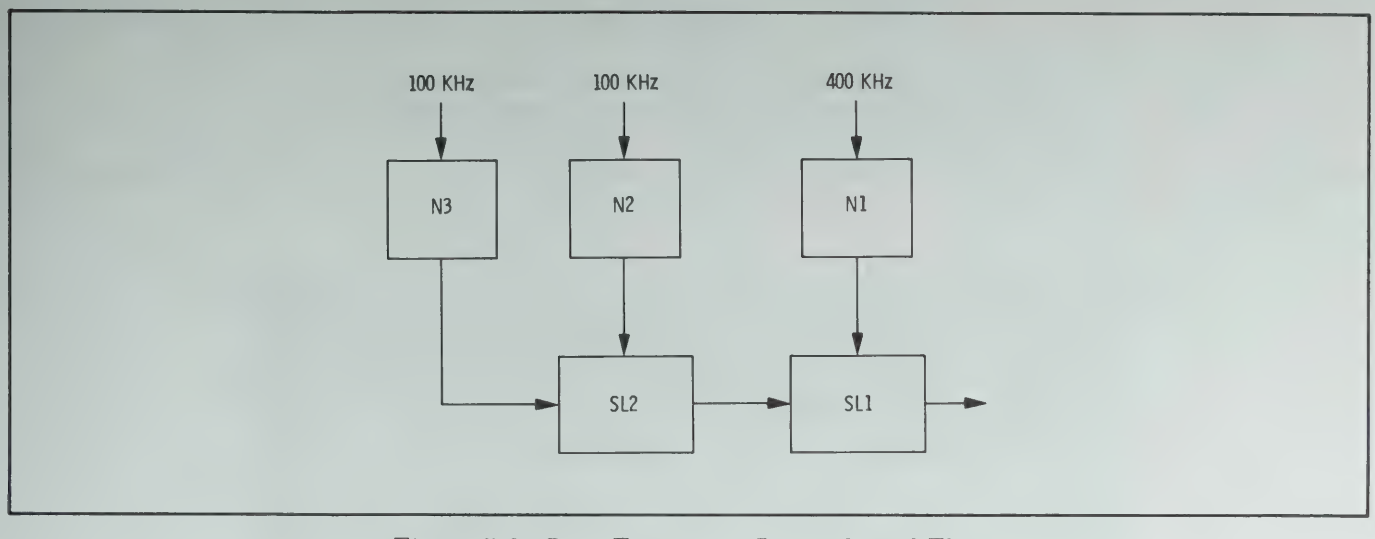


Figure 5-2. Low Frequency Loops Signal Flow

5-8. Remove the mainframe top cover. Locate the 400 kHz and two 100 kHz outputs at the front of the A4 assembly. Measure them for correct frequency with a counter, they should be accurate to 1 Hz; if all is OK, skip to paragraph 5-10. If none of the outputs are correct, check the 10.000 000 MHz input to A4A1 from A4A3.

5-9. If the 10 MHz is OK, go to Section VIII Service Sheet of the Mainframe Operating and Service Manual and repair A4A1 as required.

If the 10 MHz is defective, check the 20 MHz signal from A4A4 to A4A3. It should be exactly 20 MHz at >330 mVp-p. If OK, repair A4A3. Previous tests in paragraph 5-1 have shown that the 100 MHz reference oscillator on A4A4 is functioning properly, however, the 20 MHz circuitry may be defective.

5-10. *Checking N1.* Swing the A4 assembly up to gain access to the Mainframe Low Frequency Section motherboard A2. Refer to Appendix 3, Figure 5 and locate test point labeled *N1 Osc.* Connect the counter to that test point and program the 100 kHz and 1 MHz digits through the range from 0 through 9. See Appendix 1, Table 6 for N1 frequency vs programmed frequency. The N1 loop output should be >0.4 Vp-p.

If any of the N1 programmed frequencies malfunction, branch to the mainframe Operating and Service Manual, Section VIII, to troubleshoot circuit boards A16 and A17.

5-11. *Checking N2.* If N1 functions properly, continue to run similar tests on the N2 loop, but now vary the 100 Hz, 1 kHz, and 10 kHz digits. (1 kHz and 10 kHz for option 004 instruments). See Appendix 1 for a table of loop frequency versus programmed frequency.

If any of the N2 programmed frequencies malfunction, branch to the Mainframe Operating and Service Manual, Section VIII, to troubleshoot the N2 loop boards A14 and A13.

5-12. *Checking N3.* If an option 004 instrument is being tested, skip to paragraph 5-14. If both N1 and N2 are working OK, check the output of N3 loop at A2TP1. (See Appendix 3 for test point locations). This loop is controlled by the two least significant digits. Step these two digits from 0 through 9 and observe the loop output frequency. The frequency is shown in a table in Appendix 1. The N3 loop output should be >0.5Vp-p.

If any of the programmed frequencies malfunction, turn to Section VIII of the Mainframe Operating and Service Manual to repair A8 or A10.

NOTE

To access A2TP1, it is necessary to partially remove the DCU by removing the four screws that secure it and pushing the DCU forward. (See Figure 5-3).

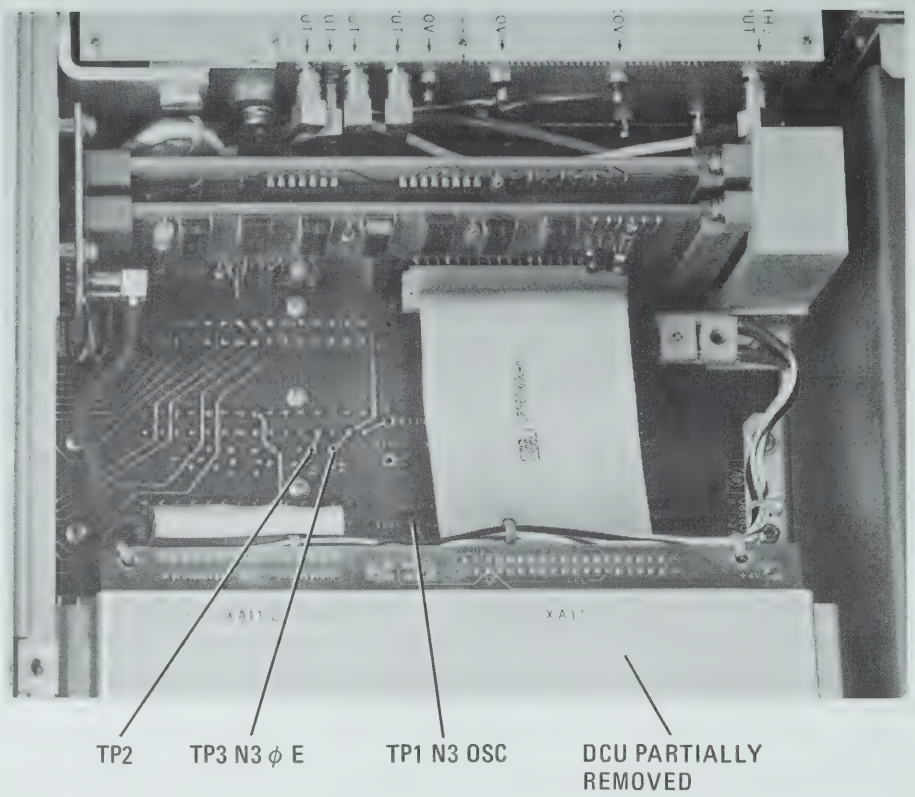


Figure 5-3. DCU Partially Removed for A2TP1 Access

5-13. *Checking SL2.* If N1, N2 and N3 all function properly (N1 and N2A in option 004 instruments), check the output of SL2 at A2TP6. (Option 004 deletes SL2).

This test point is located under the front and rear interface boards behind the DCU. Attach the probe shown to the test point without disturbing the interface boards. (See Figure 5-4).

See Appendix A for table of SL2 frequency versus programmed frequency.

The range of SL2 is 30 MHz to 20.001 MHz. If SL2 is not functioning properly, branch to the Mainframe Operating and Service Manual to repair board A11 or A12. Otherwise, the problem is in the SL1 loop, branch to the mainframe manual to repair the SL1 loop circuit boards, A15, A18, and A19.

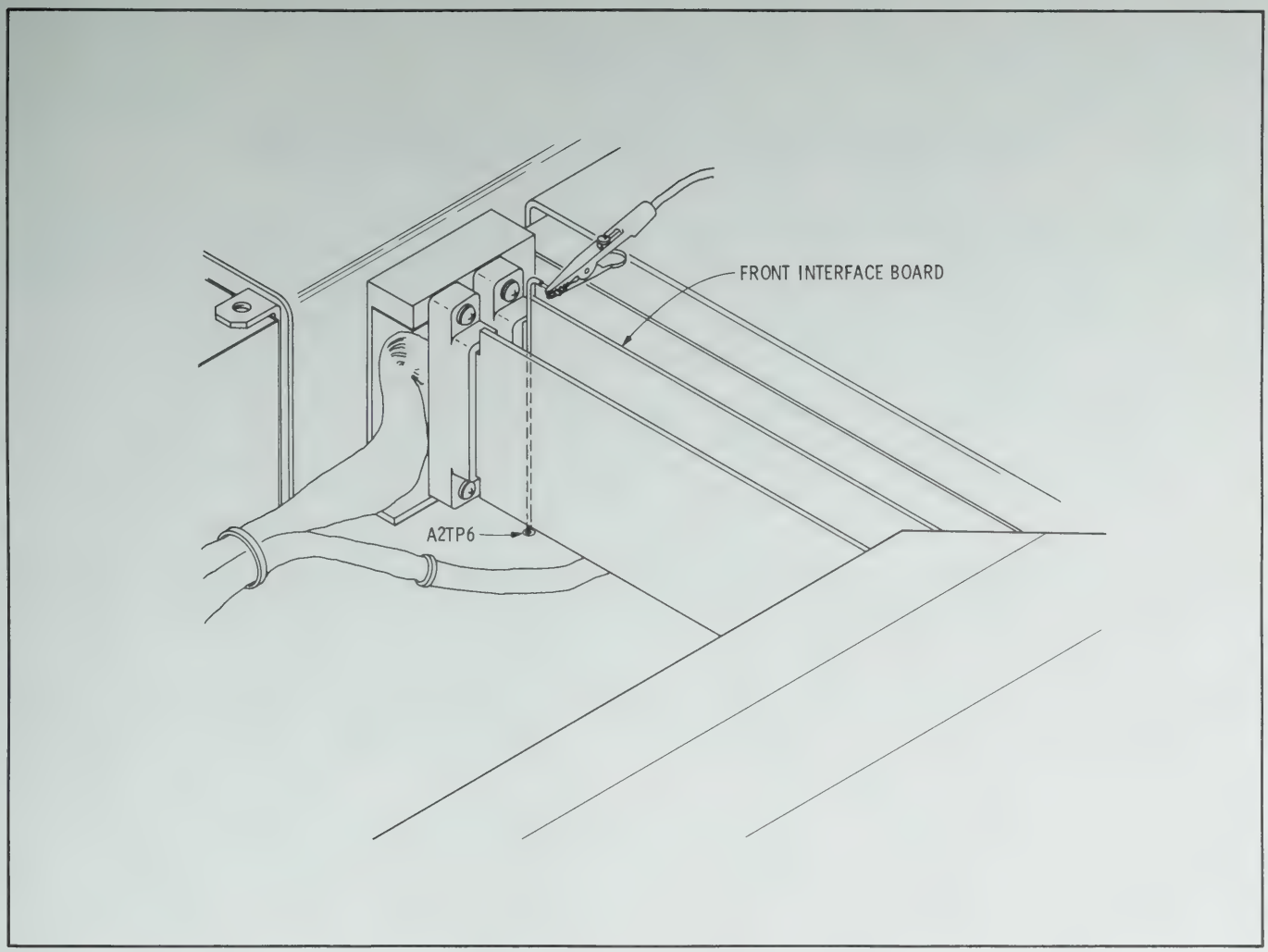


Figure 5-4. A2TP6 Access

CHAPTER 6
11661 FREQUENCY EXTENSION MODULE PROBLEMS

This section deals with problems involving the 11661 Frequency Extension Module. The 11661 contains two phase lock loops and one free running oscillator. Four phase locked signals from the Mainframe are routed to the Frequency Extension Module through the RF Section. They are:

1. 100 MHz fixed from Mainframe reference section
2. 20 MHz fixed from Mainframe reference section or 20 MHz FM from Modulation Section
3. 450-360 MHz from High Frequency Loop
4. 30 - 20.000001 MHz from SL1 loop

At the time you reach this step, all these signals should have been proven good by virtue of the tests you have made. If you skipped any steps that checked loop operation, it may be wise to go back to chech the loop that you missed since this procedure assumes proper operation of all mainframe loops.

6-1. Remove the mainframe top cover and the 11661 top cover. Locate test point 1 on the Sum Loop Phase Detector board A3. With a voltmeter or oscilloscope measure this voltage. The loop is locked if the voltage is approximately +8 to +13 Vdc. If the voltage is near +20V or near 0V the loop is unlocked.

6-2. Remove the 11661 from the mainframe and reconnect using an 11672-60002 extender cable. On the A1 assembly remove 20 MHz output cable. Connect oscilloscope to A6TP1. The voltage ramp at this test point should be about +2.5V p-p (see Figure 6-1). Adjust A7R17 so the ramp just turns on (extension modules with serial prefixes 1515A and above, use a fixed A7R17 with no adjustment necessary). Reconnect the 20 MHz output cable. The signal at A6TP1 should be 0V ±0.1V.

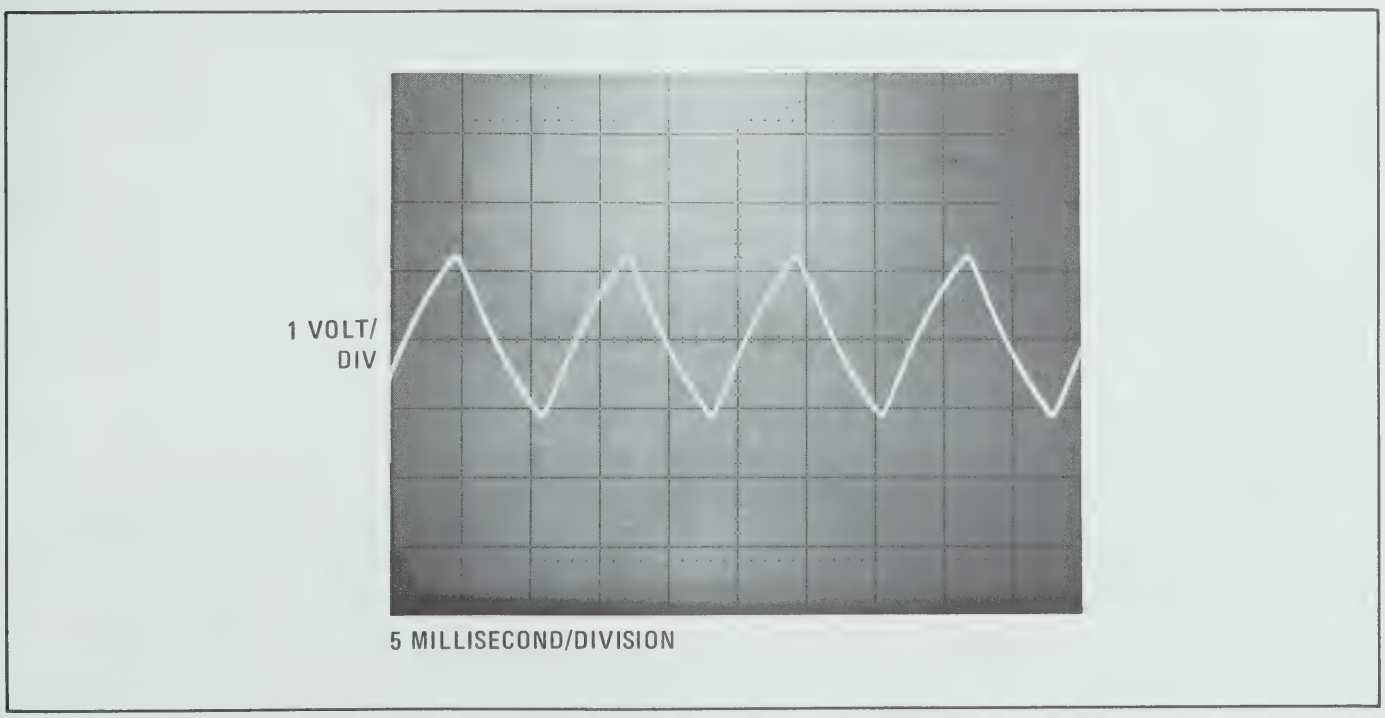


Figure 6-1. A6TP1 YIG Loop Unlocked

If the tests in paragraphs 6-1 and 6-2 indicate the loops are locked, continue with paragraph 6-3. Otherwise go to paragraph 6-5.

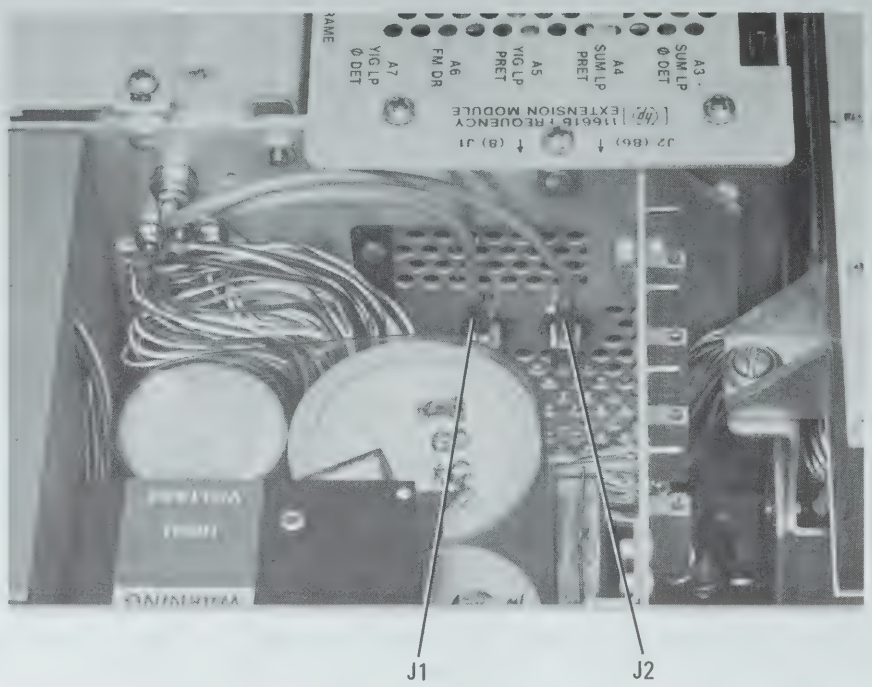


Figure 6-2. Location of J1 and J2

6-3. Turn the instrument off and unplug the mainframe from the power line and connect a microwave frequency counter to J2 (see Figure 6-2) in place of the gray/blue coax or to the 11707A 2.75-3.95 GHz output jack. Turn on the instrument and program 0000. MHz Center Frequency. Successively program zero through 1200 MHz in 100 MHz steps. The counter reading should be as shown in Appendix A Table 7, YIG loop frequency. If OK, continue, otherwise branch to paragraph 6-17.

6-4. Turn off and unplug instrument, reconnect the gray/blue coax. Connect the microwave counter to J1, Sum Loop output, in place of the gray coax or to the 11707A 3.95-4.05 GHz output jack. Turn on the instrument and program 0 through 90 MHz in 10 MHz steps. The counter reading should be as shown in Appendix A, Table 8, 11661 Sum Loop Frequency. If both sum and YIG loops program properly, connect a spectrum analyzer to the sum and YIG outputs to check their power output.

YIG Loop	J2	>+10 dBm
Sum Loop	J1	>−4 dBm

If both are OK, the 11661 is functioning properly. If the Sum Loop does not program properly, go to paragraph 6-22. If the power output is not correct, go to Section VIII of the 11661 Operating and Service Manual to repair the loop whose output is defective.

6-5. Turn off and unplug instrument, remove 11661 from mainframe (there are two retaining screws at the bottom and three at the top). Reinstall 11661 on an extender cable, HP part number 11672-60002. Connect the Microwave counter to the 4.43 GHz OUT connector A1J3 at the bottom of the 11661. Turn the instrument on and measure the oscillator frequency. It should be 4.43 GHz ± 500 kHz. *There will be some drift in the 5 least significant digits; this is normal.* If OK, continue. If 4.43 GHz is not as indicated, branch to paragraph 6-24.

6-6. *If both loops are unlocked*, check the power supplies in the 11661. If OK, continue. If not OK, check the defective voltage in the mainframe. If OK, repair interconnections and *solder* any *crimped* dc pins on the plug-in interface connectors. If not OK, branch to the Mainframe Operating and Service Manual to repair the power supply or to replace the power line module. A faulty line module can be detected by tapping the line module with the back of a screwdriver while monitoring any supply voltage. Any disturbance indicates a defective line module.

If the YIG loop is unlocked, continue to paragraph 6-7. *However, if only the sum loop is unlocked*, go to paragraph 6-28.

6-7. Turn off and unplug instrument. Remove YIG FM Driver board A6. Connect counter to J2 on rear of 11661. Turn on instrument. Program center frequency from 0 to 1200 MHz in 100 steps. The results should be as shown in Table 6-1.

Table 6-1. YIG Loop Frequencies

Center Frequency	Frequency at J2
000 MHz	3.950 GHz ± 5 MHz
100 MHz	3.850 GHz ± 5 MHz
200 MHz	3.750 GHz ± 5 MHz
300 MHz	3.650 GHz ± 5 MHz
400 MHz	3.550 GHz ± 5 MHz
500 MHz	3.450 GHz ± 5 MHz
600 MHz	3.350 GHz ± 5 MHz
700 MHz	3.250 GHz ± 5 MHz
800 MHz	3.150 GHz ± 5 MHz
900 MHz	3.050 GHz ± 5 MHz
1000 MHz	2.950 GHz ± 5 MHz
1100 MHz	2.850 GHz ± 5 MHz
1200 MHz	2.750 GHz ± 5 MHz

If the frequencies are not correct, continue with paragraph 6-8. If the frequencies are correct, go to paragraph 6-10.

6-8. Turn off instrument. Check the soldered pins on the YIG Oscillator for cold solder joints. Install the YIG Loop Pretune board A5 on an extender cable. Turn on instrument. Program 0 to 1200 MHz and check the BCD frequency data at the edge connector pins 1 through 5. This is positive logic (ON greater than 2.0V, OFF less than 0.8V). *If the data is OK*, go to paragraph 6-9. *If the data is incorrect*, unplug the A5 board and recheck the data; if still incorrect, branch to the mainframe Operating and Service Manual to repair the DCU or interface wiring. If the data is now correct, repair the A5 board.

Pin	BCD Digit Controlled
1	100 MHz
2	200 MHz
3	400 MHz
4	800 MHz
5	1 GHz

6-9. Refer to the 11661 Operating and Service Manual, Section III, and perform the Pretune Driver Assembly A5 Adjustment. If the adjustment works properly, reassemble the system and check it for proper operation. If the adjustment did not correct system operation, turn to Section VIII of the 11661 Operating and Service Manual to repair A5 or to replace the YIG oscillator *only if it proves to be defective.*

6-10. Unplug connector W4P1 20 MHz output. Attach a spectrum analyzer to the open A1A3 (20 MHz output) jack. Adjust A1C1 to peak the 20 MHz signal. The signal should be 20 MHz at ≥ -17 dBm. If OK, go to paragraph 6-11. If not OK, go to paragraph 6-13.

6-11. Turn off instrument. Reinstall board A6 and remove board A7. Turn on instrument. Attach oscilloscope to A6TP1. The signal there should be a symmetrical sawtooth 2.5Vp-p, 1.5 ms period. If OK, the problem is in A7 or A9; continue with paragraph 6-12. If not OK, repair A6.

6-12. Turn off instrument. Remove the 11661 from the mainframe and reconnect it with extender cable 11672-60002. With a 11661A, locate the 20 MHz Bandpass Filter/Amplifier can (A9) and remove the two screws holding it in place. Pull the can out far enough to remove the red output coax. With an 11661B, merely remove the two screws to allow the instrument to hinge open; it is not necessary to loosen or remove A9. Turn on instrument. Measure the signal from A9 with a spectrum analyzer or oscilloscope. Should be 20 MHz at >-6 dBm (200 mVp-p). If it is OK, repair A7 or interconnecting cables.

6-13. Set center frequency to 500 MHz. Locate and unplug the gray/green (85) coax from assembly A11 (2.6 GHz bandpass filter). The output from A11 should be greater than -8 dBm at 3.45 GHz and ≥ -10 dBm across the band of 2.75 to 3.95 GHz. If OK, go to paragraph 6-15. If not OK, continue with paragraph 6-14.

6-14. Measure the output power and frequency directly at the YIG oscillator. It should be greater than +10 dBm in the range 2.75 to 3.95 GHz. If OK, replace A11 or interconnecting cable. If not OK, check the power supply voltages to the YIG oscillator; if all are OK, replace the YIG oscillator.

6-15. Reconnect the gray/green (85) coax. Remove the A1A3 assembly cover. With a spectrum analyzer measure the output of the 4 GHz low pass filter assembly A1A3. This signal should be greater than -30 dBm in the range 480 to 1580 MHz. If not OK, go to paragraph 6-16. If OK, measure the output of the sampler A1U1; should be 20 MHz at 0.05Vp-p. If OK, repair assembly A1A1. If not OK, replace A1U1.

6-16. With the spectrum analyzer, measure the signal at the output of A1U3. It should be greater than -35 dBm in the range 480 to 1680 MHz. If OK, replace A1A3. If not OK, replace A1U3.

6-17. Turn off instrument. Remove A5 and reinstall on an extender board. Turn on instrument. Check the BCD frequency data at pins 1 through 5. The logic at these pins is positive, i.e., high = on.

6-18. If data is not OK, go to paragraph 6-20. If data is OK, follow the adjustment procedures in the 11661 Operating and Service Manual, Section III for the YIG loop, circuit boards A6 and A7. Then reprogram the frequency range while measuring the output frequency with a counter. If now OK, leave this table and return to the main Operational Tests (Chapter 2) paragraph 2-4.

6-19. If still not OK, or not adjustable, repair A7 or replace the YIG oscillator, if it proves to be defective. If it adjusts OK, but it still doesn't work, repair A5 or replace YIG oscillator if necessary.

6-20. If the data is not OK in the 11661, check the data at the DCU output with 11661 A5 unplugged.

6-21. If now OK, plug in A5 to see if data goes bad. If the data does go bad, branch to 11661 manual to repair A5. If it does not go bad when A5 is plugged in, repair the interconnecting wiring. If the data is bad at the DCU with A5 unplugged, branch to the Mainframe Manual to repair the DCU or check for a short in the interconnecting wiring.

6-22. Turn off the instrument. Extend A4 on an extender board and turn instrument ON. Check the digital BCD data to pins N, M, L, and K of the pc edge connector.

Pin N	10 MHz
Pin M	20 MHz
Pin L	40 MHz
Pin K	80 MHz

6-23. If data is OK, repair or adjust A4 as required. If data is wrong check digit 8 data at the DCU. If OK, repair interconnecting wiring. If not OK, unplug A4 and recheck data. If data now good, repair A4; if still bad, repair DCU or check for a short in the interconnecting wiring.

6-24. Check +20V supply in 11661 feeding the A1A3 4.43 GHz oscillator. The voltage should be +17V to +19 Vdc typically. If +20V supply OK and oscillator is off frequency, continue with paragraph 6-25, otherwise go to paragraph 6-27.

6-25. Adjust R1 to bring frequency to 4.43 GHz ±500 kHz. If it adjusts properly, return to the beginning of this chapter, paragraph 6-1, to recheck the phase lock loops.

6-26. If the oscillator is dead or will not adjust properly, branch to Section VIII of the 11661 Operating and Service Manual to repair A4 or replace U3 or R1 as required.

6-27. Check Mainframe +20V supply. If OK, repair interconnections *and solder any crimped connector pins*, otherwise repair the power supply.

6-28. *Sum loop unlocked.* Check Digit 8 BCD input data at pins N, M, L and K of assembly A4. If OK, continue with 6-29. If not OK, check digit 8 programming data at the DCU. If data OK at DCU, repair interconnection. If data defective at DCU, remove 11661 assembly A4. If data still defective,repair DCU or check for a short in interconnecting wiring. If data is correct with A4 removed, repair A4.

6-29. Turn off instrument. Install a TEE in the 20-30 MHz SL1 line (W8) and connect A2J1 to the TEE. This connects both inputs of A3 to SL1. A3TP1 should be within lock range (8 to 13 Vdc). If it is within this range skip to paragraph 6-30. If it is outside this range, repair A3 or the current source on A4. An easier alternate procedure involves the use of a plug-in test card details of which are given in Appendix E.

6-30. Reconnect W7P2 and disconnect W5P2. (See Appendix 3 for locations). Apply a 360 to 450 MHz signal corresponding to the mainframe loop frequency to A8J2 at +13 to +15 dBm. Is A3TP1 now in lock range?

Yes — Sum Loop Oscillator is probably bad. Refer to the 11661 Manual, Section VIII, to continue troubleshooting.

No — branch to 11661 Manual to continue troubleshooting A8.

CHAPTER 7
INTERNAL AM DEFECTIVE

7-1. Switch SOURCE to 1000 INTERNAL. If modulation is OK in this position, repair the Modulation Oscillator Assembly A5, Logic Assembly A2 or the SOURCE switch. If still not OK, continue with 7-2.

7-2. Attach an oscilloscope to the Modulation Section $\frac{\text{INPUT}}{\text{OUTPUT}}$ connector. The signal should be 1 kHz (1 millisecond period) at 280 mV peak-to-peak. If not present, repair the A5 Modulation Oscillator Assembly. If present, continue with 7-3.

7-3. Switch SOURCE to 400 Internal. Signal on oscilloscope should be 400 Hz (2.5 ms period) at 280 mV peak-to-peak. If OK, continue with 7-4. If not OK, repair the Modulation Oscillator Assembly (A5), Logic Assembly (A2) or SOURCE switch. After completing the repair, return to Chapter 2, paragraph 2-6, to complete the operational tests.

7-4. Turn off instrument. Extend the *RF Section* with its cover removed on extender cable 11672-60001. Install Reference Assembly (A9 in 86601, A10 in 86602 and 86603) on an extender board. Turn on instrument. With the oscilloscope, check pin 6 of the printed circuit edge connector. With the modulation level control turned clockwise, the signal should be approximately 2.8 Vp-p in both 400 Hz and 1000 Hz INTERNAL AM. If the signal is present here, repair the Reference Assembly in the RF Section. If the signal is not present here, the problem is most likely in the modulation section, although there could be a failure in the mainframe wiring or the RF Section connections to the Reference Assembly. Continue to paragraph 7-5.

7-5. Turn off instrument. Unplug extender cable, put RF section cover back on and reinstall the RF section in the mainframe. Install the Modulation Section with its cover removed on extender cable 11672-60002. Install the A4 Leveling Amplifier Assembly on an extender board. Turn instrument on. Set SOURCE to 400 Hz INTERNAL. With the oscilloscope, measure the signal at pin 3 of the A4 edge connector. It should be 5.5 Vp-p at 400 Hz. If OK, repair the A3 Remote Attenuation Assembly, Logic Assembly (A2) or the mainframe interconnecting wiring. If not OK, repair the A4 Leveling Amplifier Assembly or Logic Assembly (A2).

The next steps deal with the case in which 400 Hz AM works properly but 1 kHz AM is defective in some manner. Three basic failures will be covered.

1. No 1 kHz modulation. Start at paragraph 7-6.
2. Modulation present but not at 1 kHz. Go to paragraph 7-9.
3. Modulation Level incorrect. Go to paragraph 7-10.

7-6. Extend the modulation plug-in with the cover removed on an extender cable 11672-60002.

7-7. Refer to Appendix C and install the Switch Logic Assembly A2 on an extender board. Measure voltage on the following logic control lines.

Logic Control Line	Mode		
	AM INT 400	AM INT 1000	OFF
AM Control	Low	Low	High
Internal 400	Low	High	High
Internal 1000	High	Low	High

LOW = < + 0.8V HIGH = > + 2.4V

If these logic levels are correct, the problem is on the modulation oscillator board, or the mother board. Use the schematic and troubleshooting information in the Operating and Service Manual to repair.

7-8. If any control line is always low, unplug the circuit board which contains the controlled components. If the line now functions properly, repair the board you removed. Otherwise, repair the logic control board or the front panel switches or cabling.

7-9. Modulation present but not at 1 kHz. This is definitely a Modulation Section problem. Branch to Section VIII of the Modulation Section, Operating and Service Manual to repair the modulation oscillator or switch logic boards as required.

7-10. Modulation level incorrect at 1 kHz. Definitely a modulation section problem. Probably in Switch Logic, Modulation Oscillator or Remote Attenuation Assembly. Branch to Section VIII of the Modulation Section, Operating and Service Manual to repair as required.

CHAPTER 8
FM MALFUNCTIONS

8-1. Remove the modulation section's cover and connect the section to the mainframe with an extender cable HP part number 11672-60002.

8-2. Switch SOURCE switch to 400 Hz INTERNAL. Attach oscilloscope to A3 Test Point 1. Should measure 2.8 Vp-p at 400 Hz with MODULATION LEVEL control turned to maximum clockwise. If OK, continue with paragraph 8-3. If not OK, go to paragraph 8-6.

8-3. Fold the 20 MHz Oscillator assembly back and connect a spectrum analyzer to the OUT jack in place of the gray/red (82) coax. Vary the MODULATION LEVEL control and MODE switch to cover all FM positions. If operation not OK, continue to paragraph 8-4. If operation is OK, check the 20 MHz interconnections through the mainframe and into the RF section or Frequency Extension Module.

8-4. Measure FMC line at the feedthrough into the 20 MHz oscillator assembly. It should be logic low for all FM modes. If OK, continue with paragraph 8-5. It not OK, unplug the switch logic board and check the FMC line for a short to ground. If FMC is not shorted, repair the switch logic board or mother board, or FM CF CAL circuitry (see Chapter 9 for troubleshooting).

8-5. Check the DC lines feeding the 20 MHz oscillator. If OK, repair the oscillator assembly (A7A1, A7A2, or A7A3). If not OK, repair the power supply interconnections.

8-6. With an oscilloscope, measure A5TP1. Should be 2.6 Vp-p at 400 Hz. If not OK, repair A5; if OK continue.

8-7. Extend A4 Leveling Amplifier and measure the signal at pin 3 with the oscilloscope. Should be 5.5 Vp-p at 400 Hz. If OK, repair board A3, Remote Attenuation Assembly. If not OK, repair the A4 Leveling Amplifier.

CHAPTER 9
FM CENTER FREQUENCY CALIBRATE BUTTON MALFUNCTIONS (86632 AND 86635 ONLY)

NOTE

If the center Frequency Calibration Cycle intermittantly self-initiates, request a copy of Service Note P-08660-60273 from your nearest HP Sales Office and do the modification recommended in Section 4 of that note.

FM CF CAL affects four assemblies in the 86632 and 86635.

1. It grounds the modulation input on the A3 Remote Attenuation board.
2. It closes the phase error feedback path on the A7A3 20 MHz VCO board.
3. It ungrounds the A7A1 phase detector reference input and connects it to the 20 MHz mainframe reference signal.
4. It causes the FM UNCAL line to go high on the A2 Switch Logic board, (which turns off the mainframe front panel FM lamp).

9-1. Turn off instrument. Extend the 86632 or 86635, with cover removed, on extender cable 11672-60002.

9-2. Remove the A6 FM Deviation Attenuation board and reinstall it on an extender board. Turn the instrument on.

9-3. With a voltmeter measure pin 11 on the A6 edge connector. This signal should be a logic high (approximately 5 Vdc). If OK, continue with paragraph 9-4, if not OK, go to paragraph 9-10.

9-4. Press the front panel FM CF CAL button. Pin 11 should go low for approximately 5 seconds. If not OK, repair A6 or mother board interconnections.

9-5. If OK, repeat the same test pins 9, 10 and 12. If any are bad, repair A6. If all are good, continue.

9-6. Turn instrument off, reinstall A6 in its normal position. Extend the A2 switch logic board and turn instrument on.

9-7. Measure pin 10 of the A2 edge connector. It should be logic high. Press the CF CAL pushbutton. Pin 10 should go low for 5 seconds. If OK, continue. If not OK, repair A2 or the mother board interconnection.

9-8. Turn off instrument. Reinstall A2 . Remove A3 and install on an extender board. Refer to Service Sheet 5, Section VIII, of the 86632 or 86635 Operating and Service Manual to locate relay A3K13. Turn on instrument, check operation of A3K13. If OK, continue; if defective, repair as required.

9-9. Turn off instrument. Reinstall A3. Fold A7 assembly back and remove the A7A1/A7A2 cover. Turn on instrument. Refer to Service Sheet 7 in the 86632 or 86635 manual to check operation of the relays on A7A2. If defective, repair A7A2 on the connecting control lines. If OK, carefully check the operation of the error voltage circuitry on A7A3.

CAUTION

Damage to A7A3Q7 may occur if anything except a ground clip is connected to the teflon insulated standoff on A7A3.

CHAPTER 10
EXTERNAL MODULATION DEFECTIVE (INTERNAL OK)

This chapter deals with external modulation malfunctions *when all internal modulation is working properly.*

10-1. Turn off instrument. Install the modulation section, with its cover removed, on an extender cable 11672-60002. Install the leveling amplifier board (A4) on an extender. Turn on instrument. Connect external modulation source to INPUT/OUTPUT connector at 1.8 Vrms. SOURCE switch to EXTERNAL AC.

10-2. With an oscilloscope check the signal at pin B of the A4 edge connector. If the voltage is 1.8 Vrms (5.1 Vp-p), the external AC is working properly; continue with paragraph 10-3. If not OK, go to paragraph 10-5.

10-3. Switch to EXTERNAL DC. The signal should be 1.8 Vrms at pin B of A4 edge connector. If OK, the external input circuitry is working properly. If not OK, continue with paragraph 10-4.

10-4. Measure the signal at pin 10 of the A4 edge connector. Should be 1.8 Vrms. If OK, repair A4 or its associated control circuitry. If not OK, repair A5, A2 or input cabling.

10-5. Measure the signal at pin N of the A4 edge connector. If OK, repair A4 or associated control circuitry. If not OK, repair A5 or associated control circuitry.

CHAPTER 11
PHASE MODULATION MALFUNCTIONS

This chapter deals with phase modulation malfunctions both in the modulation sections and in the RF section.

11-1. Remove RF Section from mainframe and replace it with the 11707 Test Plug-in.

11-2. Switch DC/MOD OUTPUT on 11707 to ϕM. Attach oscilloscope or AC voltmeter to the DC/MOD output jack.

If an 11707 is not available, the signal can be accessed at mainframe J6 pin 59. This is a coaxial pin. Use HP Part Number 11672-60008 adapter to connect to the pin without damage. Set Modulation section to ϕM 400 Hz INTERNAL. Set Mainframe center frequency to 100 MHz. Set MODULATION LEVEL for 100 ° (full scale). The voltage out of the 11707 should be 1.5 Vrms ± .03 Vrms (4.24 Vpp ± .08 Vpp). The Modulation Section meter should read full scale (±5%); the REDUCE DEVIATION lamp should not be on. Set center frequency to 1400 MHz. Set MODULATION LEVEL for 200° (full scale). The output voltage should be 1.5 Vrms as above.

11-3. If all is OK to this step, the modulation section's phase modulation circuitry is functioning. Skip to step 11-8. If some portion is not working properly, extend the modulation section with its cover removed on extender cable HP Part Number 11672-60002.

11-4. Measure the output of the MODULATION OSCILLATOR assembly.

Model	Assembly	Test Point	Voltage
86634	A2	Motherboard OUTPUT test-point.	3.4 Vp-p
86635	A5	A5TP1	2.6 Vp-p

If OK continue. If not OK, go to Modulation Section Operating and Service Manual Section VIII to troubleshoot the modulation oscillator.

11-5. If troubleshooting an 86634, go to the Operating and Service Manual, Section VIII, to troubleshoot the A2 Amplifier Assembly.

11-6. With an 86635, measure the output of A3 Remote Attenuation Assembly. Should be 0-1 Vrms at A3 edge connector pin M for center frequencies below 1300 MHz and 0—0.5 Vrms for frequencies 1300 MHz or above.

11-7. If this voltage is correct, go to Section VIII of 86635 Operating and Service Manual to troubleshoot A9 Deviation Detector Assembly. If the voltage is not correct, troubleshoot A3 Remote Attenuation Assembly.

11-8. Remove the 11707 Test Plug-In and install the 86603 RF Section with its covers removed on an extender cable, HP Part Number 11672-60001. Set the modulation section for full scale phase modulation. Disconnect the cable connecting the A16 Phase Modulator Driver Assembly to the A17 Phase Modulator Assembly. Measure the drive voltage from A16 on an oscilloscope. It should be ~7.5 Vdc

plus 7.5 Vp-p when the modulation section is set for 100° modulation index below 1300 MHz or 200° modulation index 1300 MHz or above. The DC level is fixed; the AC level determines the modulation index.

11-9. If the output of A16 is OK, the Phase Modulator Assembly, A17, or the interconnections to the Circulator Assembly, A18 is defective. The operation of the Circulator may be tested by measuring the forward insertion loss from J1 to J4. The loss should be about 6 dB when A18J2 and A18J3 are properly terminated in the Phase Modulator Assembly

CHAPTER 12
8660B/C TROUBLESHOOTING USING ASM FLOWCHARTS

GENERAL DESCRIPTION

The 8660B and 8660C DCU (Digital Control Units) uses a form of sequential logic known as an Algorithmic State Machine (ASM). The actual ASM is really only two assemblies of the ten in the DCU. The other assemblies process data and are controlled by signals from the ASM. The ASM assumes a series of states. Each state is denoted by a 7-bit binary number. For convenience this binary number is decoded as two decimal numbers by grouping together the right four bits and left 3 bits, i.e., 101 1011 would be 5/11. Every state has a unique set of output signals called instructions which are active during that state. The number of instructions in this set can be zero or any number. These signals control other DCU logic circuits which process data.

The sequence of states which the ASM assumes depends on what action is to be performed. Generally the ASM goes from the state it's in to one of two possible next states. An input signal to the ASM called a qualifier determines which of the two possible next states the ASM will go to. Qualifiers are generated in the DCU logic and represent the status of some event or process in the DCU. For example, pushing a key on the front panel generates some qualifiers to tell the ASM what has happened.

The seven bit state number is stored in seven flip-flops on the A4 assembly. LED's are mounted on the top edge of the board and display the state number stored in the flip-flops. In normal operation the ASM goes from one state to the next at a one MHz rate. You can disable this clock and step the ASM from state to state by pushing a switch on the top edge of A4. You can stop at each state as long as desired to measure qualifiers and instructions or read the state number on the LED's.

The operation of the ASM is best described by a flow chart. Figure 1 is a section of the 8660C flow chart. The rectangular boxes represent the states which the ASM assumes. The state number is in the upper left hand corner of the rectangle.

The mnemonics inside the rectangles are instructions which are active during that state. The mnemonic convention used in the 8660B/C is that all mnemonics end with —L or —H which defines the active state of the signal as low or high. In states where the signal [RKD2, KF10]-H is active, the signal is high. In all other states it is low. Two mnemonics in brackets means that there is only one signal but it performs two functions. Each mnemonic refers to one of the functions. In the troubleshooting flow charts below each mnemonic is information describing where that signal originates and where it goes, i.e., in the example A5→A2,A1 the signal originates on A5 and goes to A2 and A1. There are mnemonic information tables in the 8660B (Table 8-2) and 8660C (Table 8-4) manuals which may be helpful in explaining what a mnemonic means.

The mnemonics inside the diamond shaped symbols denote qualifiers. There are two branches from the symbol. If the qualifier is low in Figure 1, the ASM will go to state 4/1, otherwise, the qualifier is high and the ASM goes to state 0/5. The qualifier is an input to the ASM. All qualifiers go into a multiplexer on the A4 board and the ASM addresses this multiplexer to select the qualifier (if any) that will be checked in each state.

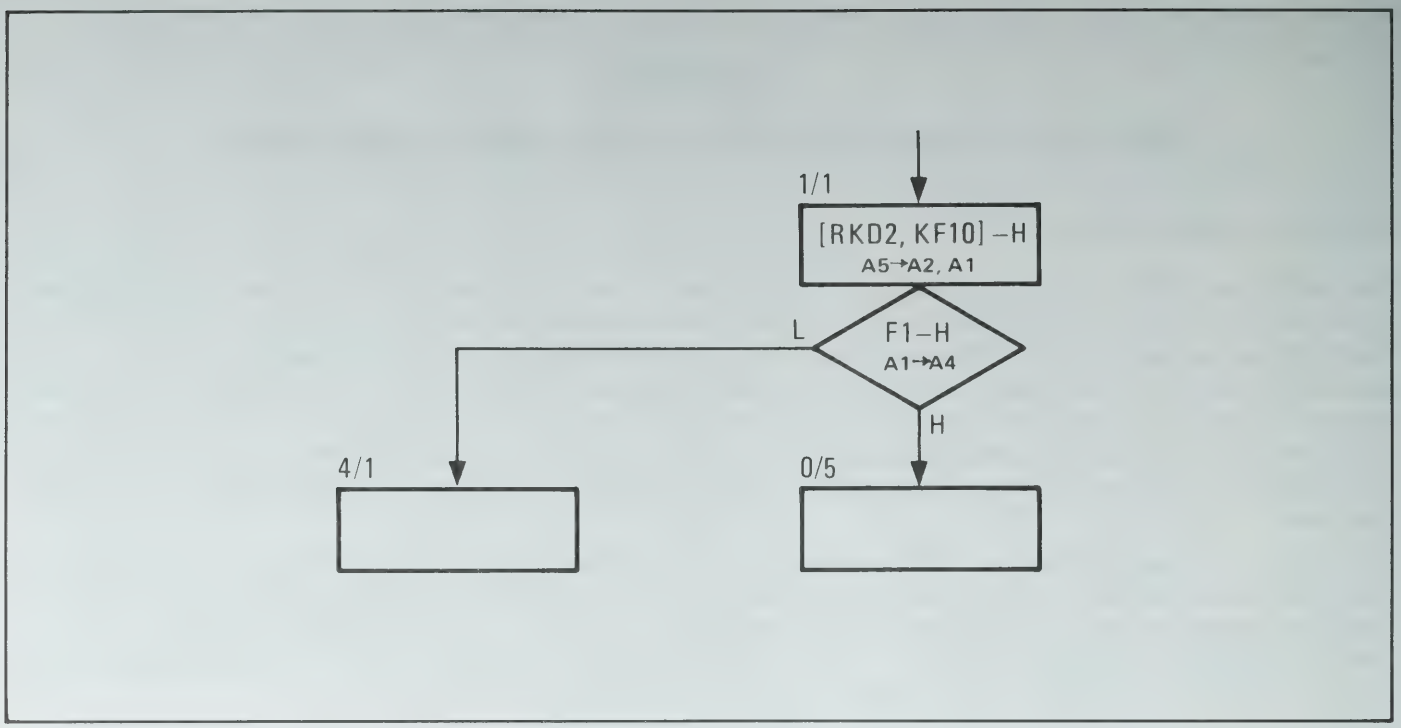


Figure 12-1. ASM Flow Chart Example

TROUBLESHOOTING

The ASM flow chart is a very powerful troubleshooting tool. Troubleshooting flow charts in this chapter provide detailed information about the ASM state sequence for specific DCU operations. These charts specify the state of every qualifier and describe qualifiers and data flow for specific DCU operations.

In order for the DCU to operate properly , the following conditions must be met:

1. The ASM must go through the proper state sequence. This requires that all qualifier circuitry is operating correctly.

2. The ASM must generate the correct instructions which go to the data processing circuitry.

3. The data processing circuitry must perform the proper action when it receives an instruction from the ASM.

Each condition can be met only if all those above it are met. This fact leads to a logical method of troubleshooting the DCU.

1. The area of trouble must be localized. This can best be done by using the DCU Block Diagram in the 8660B/C Operating and Service Manuals.

2. Confirm that the ASM is going through the proper sequence by using the troubleshooting flow charts. This verifies condition (1), above, which is a necessary but not a sufficient condition for DCU operation.

Two ways of checking the ASM are to single-step using the pushbutton on the A4 assembly, or to use a logic analyzer to dynamically monitor the ASM operation. The logic analyzer is the better method. The state flip-flops on the A4 board can be monitored as well as any instructions or qualifiers of interest.

Single-stepping can be done by following the HOW TO USE instructions included with every troubleshooting flow-chart.

3. If the flowchart sequence is correct, verify that the proper signals are output from the ASM. This verifies condition (2).

4. If the output signals from the ASM are correct, check that the data processing circuitry is correct. This can be done by checking that the data moves from register to register as it should. Logic diagrams of the IC's used in the registers are contained in Figure 12-2.

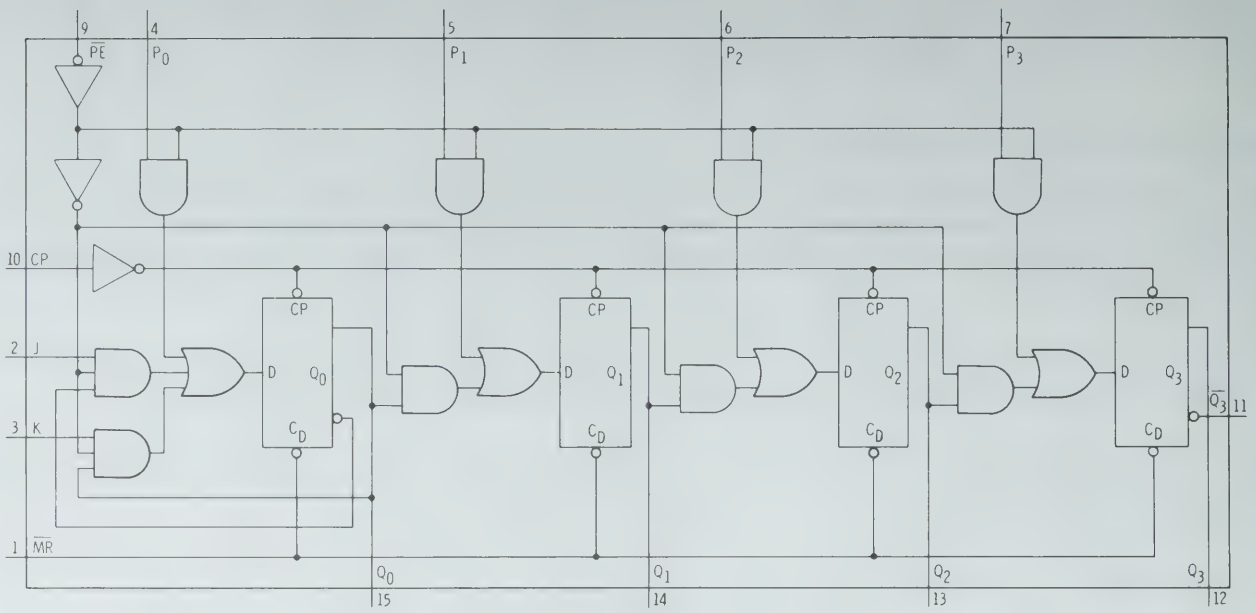
TROUBLESHOOTING FLOW CHARTS

Figures 12-3 through 12-12 are troubleshooting flow charts for the most common DCU operations. These charts specify in what states qualifiers and instructions should be for specific DCU operations. Each chart is really a subset of the main DCU Algorithmic State Machine Flow Graph in the 8660B and 8660C Operating and Service Manuals.

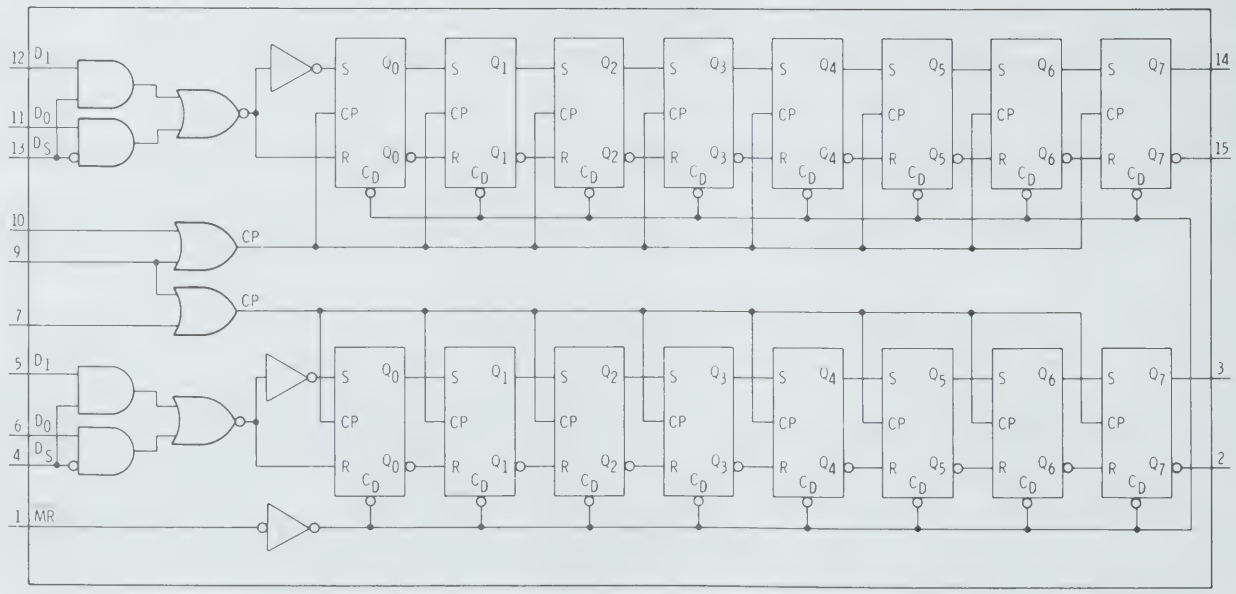
Table 12-1 and 12-2 describe the operation of flip-flops and counters which affect and are affected by the ASM. These tables provide more details of operation than can be described on the flow charts.

All flow chart sequences start with state 0/0 and end with state 0/0. The starting point on each chart is the upper left hand corner. The end of each sequence is on the right hand edge of the chart when state 0/0 is reached. This state 0/0 is the same state at which the sequence was started.

There is one difference between using the single-step pushbutton and the logic analyzer. Putting the DCU in manual mode causes the state flip-flops to be clocked by the MAN SW pushbutton, however, the data registers in the DCU are still clocked by the DCU clock. There are many states where data is transferred from one register to another which takes 10 clock pulses. States 1/12 and 2/5 in figure 12-6 are examples. When using the logic analyzer, you would see the ASM staying in each of these states for 10 clock pulses. When using the MAN SW pushbutton, pushing the button moves the ASM from state 5/7 to state 1/12. Pushing the button again moves the ASM to state 2/2. When state 1/12 was reached, the data was transferred by the next 10 pulses of the system clock. Thus the qualifier was satisfied when the pushbutton was next pressed and the ASM appeared to stay in state 1/12 for only one clock pulse.



4 BIT SHIFT REGISTER
HP P/N 1820-0659, TYPE 93L00



DUAL 8 BIT SHIFT REGISTER
HP P/N 1820-0709, TYPE 93L28

Figure 12-2. Logic Diagram of IC's Used in DCU Shift Registers

Table 12-1. Flip-Flops Used as ASM Qualifiers (1 of 2)

Mnemonic	Ref Designator A1*	Description
CFR	A1U10B (B) A1U11B (C)	This flip-flop is set during state 3/6 after one of the read-out control buttons is pressed. CFR stays set when the button is first released and is cleared when state 1/8 is reached.
F1	A1U15A(B) A1U16A(C)	Interrupt flip-flop. Set in state 0/10 when a keyboard entry, a manual entry, or a push-button entry is made during a sweep operation. Reset in state 0/5 while the entry is being made.
F2	A4U16B	Initial entry flip-flop. Set when a units key is pressed (state 0/6) or when an entry key is pressed (state 0/7). Reset by first numeric entry (state 1/5) after being set. Used so the keyboard can be reset at the start of each new entry operation.
F3	A2U7B	Prevents an entry operation from being made before a units key is pressed. F3-L is active when the flip-flop is reset which means a units key has been pressed. Reset in state 1/6 when a units key is pressed. Set by states 1/11, 1/12, 1/13, or 1/0. Also set if CLEAR KYBD key is pressed.
F7	A4U16A	This flip-flop is set when sweep mode is entered during state 0/13. It remains set during sweep mode and is reset when leaving sweep mode during state 2/9. Also set under certain conditions during remote mode.
F8	A4U15A	Sweep ramp qualifier flip-flop. Used in sweep mode. When not set, prevents the RF output of the 8660 from changing by preventing the frequency steps calculated in the DCU from being sent to the output register. Not set when sweep mode is first entered during the time the digital frequency data is stepped from the beginning center frequency to the upper frequency in the sweep range at maximum rate. Set when the data is at the maximum frequency during state 2/15 and remains set until leaving sweep mode during state 2/9.
F9	A1U21B(B) A1U23B(C)	Determines how fast the DCU steps the frequency data (the time between steps). Selects either the system clock rate (1 MHz) or the rate determined by the setting of the Sweep Rate Switch. The QSP flip-flop is clocked at the rate determined by F9. F9 is normally reset allowing the setting of the Sweep Rate switch to determine the time between steps. There are three conditions when F9 is set: 1) When sweep mode is entered, while the data is stepped from the beginning center frequency to the upper frequency of the sweep range. 2) When the sweep range exceeds the upper limit of the RF plug-in being used. Once an illegal frequency is stepped to, F9 is set in state 0/15 and the frequency data is stepped to the upper limit at system clock rate. 3) When part of the sweep range is below zero. When the frequency data is negative, F9 is set in state 0/14 and the frequency data is stepped to zero or above at the system clock rate. When each of these conditions no longer exists, F9 is cleared in state 0/9.
F10	A1U15B(B) A1U16B(C)	Start flip-flop. When a keyboard entry, manual tune entry, pushbutton entry or sweep operation is initiated, F10 is set. A remote programming entry also sets F10. F10 must be set before the ASM can leave state 0/0.
IUP IDN	A4U14B A4U14A	These flip-flops inhibit sweep up and inhibit sweep down when in manual sweep mode if set. They are set and cleared by instructions from the ASM when the sweep counter on A1A8 reaches its maximum count or zero.

Table 12-1. Flip-Flops Used as ASM Qualifiers (2 of 2)

Mnemonic	Ref Designator A1 *	Description
KD2	A2U17A	This flip-flop is set whenever a key is pressed (KDN-H made active) or CMND-P from the A3A1 interface assembly goes low in remote mode. The KD2-L output is one of the inputs which can cause the F10 flip-flop to be set.
MNE	A1U29A(B) A1U32A(C)	Turning the manual tune knob on the front panel in either direction sets this flip-flop in manual sweep mode or manual tune mode.
QB	A7U19A	This flip-flop is set whenever the two digits being added generate a carry and cleared if a carry is not generated. Thus when a 10, 12, or 13 digit number is added, this flip-flop will be set or cleared for each operation but will retain the state for the last operation. There are two situations where add or subtract operations leave QB set. 1) When subtracting two numbers that gives a result less than zero. Trying to STEP↓ an amount greater than the center frequency is an example. 2) When the frequency data is a negative number and a number is added to it making the new frequency a positive number. This happens when the sweep width is greater than twice the center frequency. Part of the sweep range would thus be negative numbers. The QB flip-flop is set when the lowest frequency is calculated which generates a negative number. Sweep width increments are added to this number, but as long as the result is still a negative number QB is not set again. At a certain point the result will be zero or greater and this operation will set QB.
QSP	A1U14B(B) A1U15B(C)	QSP flip-flop. This flip-flop is periodically set at a rate determined by the SWEEP SPEED switch and flip-flop F9. After adding a step to the output frequency the ASM goes into a wait loop between 3/14 and 0/10 until QSP is set. Then it adds another step to output frequency and returns to the wait loop. Thus the rate at which QSP is set determines how fast the sweep occurs.
SW1	A1U21A(B) A1U23A(C)	Both these flip-flops are set for all sweep operations.
SWON	NONE (B) A1U28A(C)	
ZER	A7U19B	Used only in sweep mode and can be set only in state 2/14. When QB is set because the lower frequency limit of the sweep range is a negative number, ZER is set and remains set until the frequency data becomes zero or greater.

*If the designators are different for the 8660B and 8660C, both designators are listed.

Table 12-2. Explanation of Counters

Name	Ref Designator	Description
Encode Counter	A7U2	Used in manual tune mode and power on initialization to address ROM #4 (A7U9) which outputs the manual-tune increments which are added to the data from the R bus. For power-on initialization ROM #4 puts out 0 001 000 000 (1 MHz, same as the course tune increment) which is added to the center frequency data which is all zeros because the register has been cleared. The result is 1 MHz which goes into the center frequency register.
Justification Counter	A3U20	This counter controls the justification operation. Refer to the circuit description of Service Sheet 23 in the 8660B or 8660C Operating & Service Manual for an explanation.

PRESSING NUMER

ANY KEY ON THE KEYBOARD
HE F10-H SIGNAL TO BECOME
HIS SIGNAL STAYS ACTIVE AS
HE KEY IS HELD DOWN.

The keyboard decodes the key which is pre
sents that key. When state 0/2 is reached,
During state 0/3 the K0 register and the Ke
the right. This moves the number which w
shift register. All the other numbers in the
their previous position. Every time a key i
shifting insures that the least significant dig
when the keyboard register data is shifting

TIVE ONLY IN SWEEP MODE
OTE MODE.

HOW

1. Turn the LINE switch to STBY and t

TIVE WHEN THE DECIMAL POINT
NG HELD DOWN.

2. Ground the DCU MAN TP momentar

3. Press a numeric key and hold pressed

4. Single step the ASM using the MAN S
chart.

ACTIVE WHEN A NUMERIC KEY
OWN.

TIVE THE FIRST TIME A KEY IS
OLLOWING A PREVIOUS ENTRY
N OR FOLLOWING POWER

F2 (A4U16B), KEYBOARD AND
TION FLIP-FLOP (A3U14A)
T.

ACTIVE WHEN A NUMERIC KEY IS
NN.

RESENTING THE KEY PRESSED IS
INTO THE K0 REGISTER ON A2.

EGISTER AND KEYBOARD SHIFT
ARE SHIFTED BY 10 CLOCK
THIS PUTS THE DATA THAT WAS IN
HE RIGHT END OF THE SHIFT
.

ECOMES ACTIVE AFTER 10 CLOCK
HAVE OCCURRED. EACH CLOCK
HIFTS THE DATA ONE PLACE TO
HT.

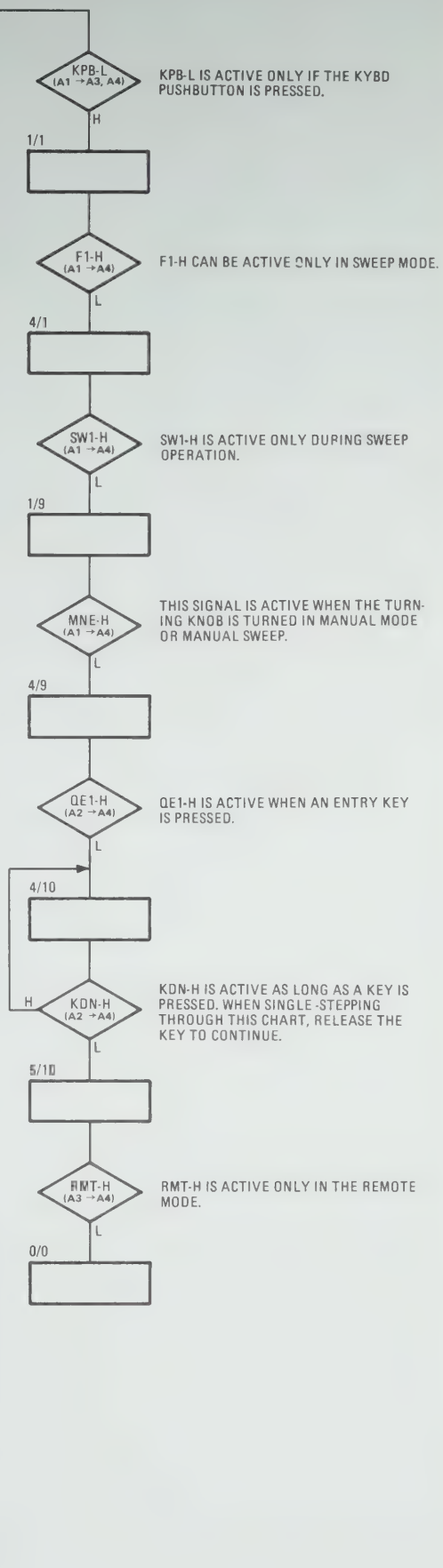


Figure 12-3. ASM Troubleshooting Flow Chart for Numeric Key Pressed

Table 12-1. Flip-Flops Used as ASM Qualifiers (2 of 2)

Mnemonic	Ref Designator A1 *	Description
KD2	A2U17A	This flip-flop is set whenever a key is pressed (KDN-H made active) or CMND-P from the A3A1 interface assembly goes low in remote mode. The KD2-L output is one of the inputs which can cause the F10 flip-flop to be set.
MNE	A1U29A(B) A1U32A(C)	Turning the manual tune knob on the front panel in either direction sets this flip-flop in manual sweep mode or manual tune mode.
QB	A7U19A	This flip-flop is set whenever the two digits being added generate a carry and cleared if a carry is not generated. Thus when a 10, 12, or 13 digit number is added, this flip-flop will be set or cleared for each operation but will retain the state for the last operation. There are two situations where add or subtract operations leave QB set. 1) When subtracting two numbers that gives a result less than zero. Trying to STEP↓ an amount greater than the center frequency is an example. 2) When the frequency data is a negative number and a number is added to it making the new frequency a positive number. This happens when the sweep width is greater than twice the center frequency. Part of the sweep range would thus be negative numbers. The QB flip-flop is set when the lowest frequency is calculated which generates a negative number. Sweep width increments are added to this number, but as long as the result is still a negative number QB is not set again. At a certain point the result will be zero or greater and this operation will set QB.
QSP	A1U14B(B) A1U15B(C)	QSP flip-flop. This flip-flop is periodically set at a rate determined by the SWEEP SPEED switch and flip-flop F9. After adding a step to the output frequency the ASM goes into a wait loop between 3/14 and 0/10 until QSP is set. Then it adds another step to output frequency and returns to the wait loop. Thus the rate at which QSP is set determines how fast the sweep occurs.
SW1	A1U21A(B) A1U23A(C)	Both these flip-flops are set for all sweep operations.
SWON	NONE (B) A1U28A(C)	
ZER	A7U19B	Used only in sweep mode and can be set only in state 2/14. When QB is set because the lower frequency limit of the sweep range is a negative number, ZER is set and remains set until the frequency data becomes zero or greater.

*If the designators are different for the 8660B and 8660C, both designators are listed.

Table 12-2. Explanation of Counters

Name	Ref Designator	Description
Encode Counter	A7U2	Used in manual tune mode and power on initialization to address ROM #4 (A7U9) which outputs the manual tune increments which are added to the data from the R bus. For power-on initialization ROM #4 puts out 0 001 000 000 (1 MHz, same as the course tune increment) which is added to the center frequency data which is all zeros because the register has been cleared. The result is 1 MHz which goes into the center frequency register.
Justification Counter	A3U20	This counter controls the justification operation. Refer to the circuit description of Service Sheet 23 in the 8660B or 8660C Operating & Service Manual for an explanation.

PRESSING NUMERIC KEY DATA FLOW

The keyboard decodes the key which is pressed and generates the BCD code which represents that key. When state 0/2 is reached, this BCD number is latched into the K0 register. During state 0/3 the K0 register and the Keyboard Shift Register are shifted 10 places to the right. This moves the number which was in the K0 register to the right end of the shift register. All the other numbers in the shift register end up one place to the left of their previous position. Every time a key is pressed this entire sequence is repeated. This shifting insures that the least significant digit is shifted out of the keyboard register first when the keyboard register data is shifting into other registers in the DCU.

HOW TO USE

1. Turn the LINE switch to STBY and then to ON to initialize the instrument.
2. Ground the DCU MAN TP momentarily.
3. Press a numeric key and hold pressed in.
4. Single step the ASM using the MAN SW and check using the troubleshooting flow chart.

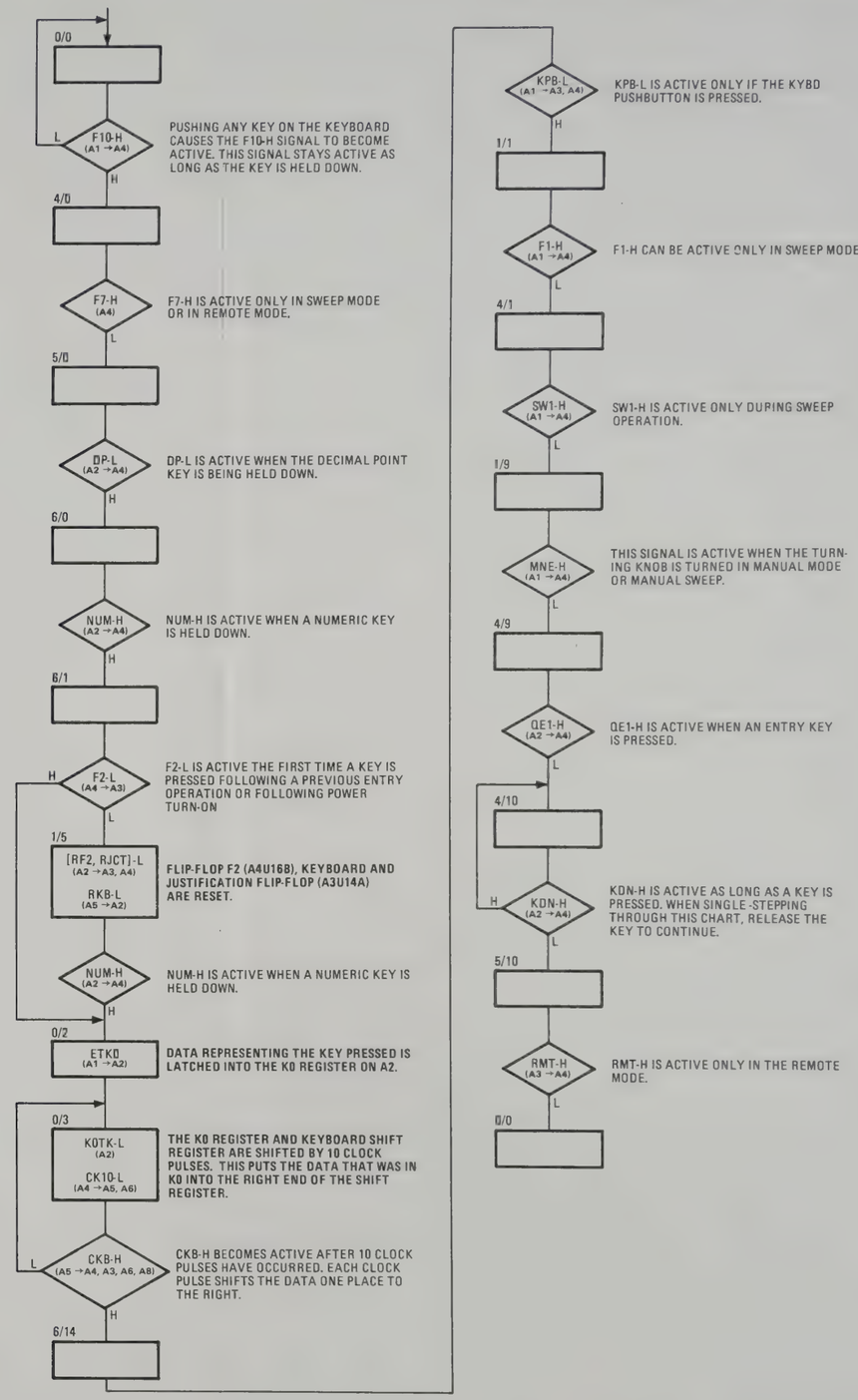


Figure 12-3. ASM Troubleshooting Flow Chart for Numeric Key Pressed

DECIMAL POINT KEY

The keyboard decodes the key pressed. W
on A3 is set. This enables the justification
are pressed. Justification means shifting th
mal point is in the right place for the units
out Control Assembly. The circuit descrip
tains a good description of the justificatior

HOW

1. Turn the LINE switch to STBY and t
2. Press the "1" key and release.
3. Ground the DCU MAN TP momentar
4. Press the decimal point key and hold
5. Single step the ASM using the MAN S

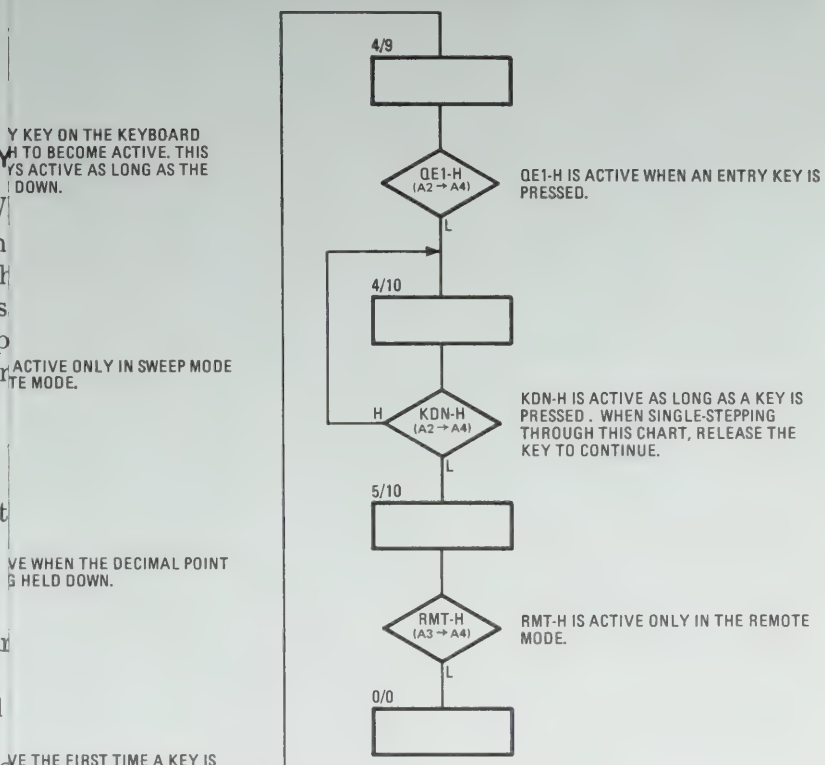


Figure 12-4. ASM Troubleshooting Flow Chart for Decimal Point Key Pressed

DECIMAL POINT KEY PRESSED DATA FLOW

The keyboard decodes the key pressed. When state 3/5 is reached, the justification flip-flop on A3 is set. This enables the justification counter on A3 to be clocked when numeric keys are pressed. Justification means shifting the data in the keyboard shift register so the decimal point is in the right place for the units selected. Justification takes place on the A3 Readout Control Assembly. The circuit description for this assembly in the 8660 manual contains a good description of the justification operation.

HOW TO USE

1. Turn the LINE switch to STBY and then to ON to initialize instrument.
2. Press the "1" key and release.
3. Ground the DCU MAN TP momentarily.
4. Press the decimal point key and hold pressed in.
5. Single step the ASM using the MAN SW and check using the troubleshooting flow chart.

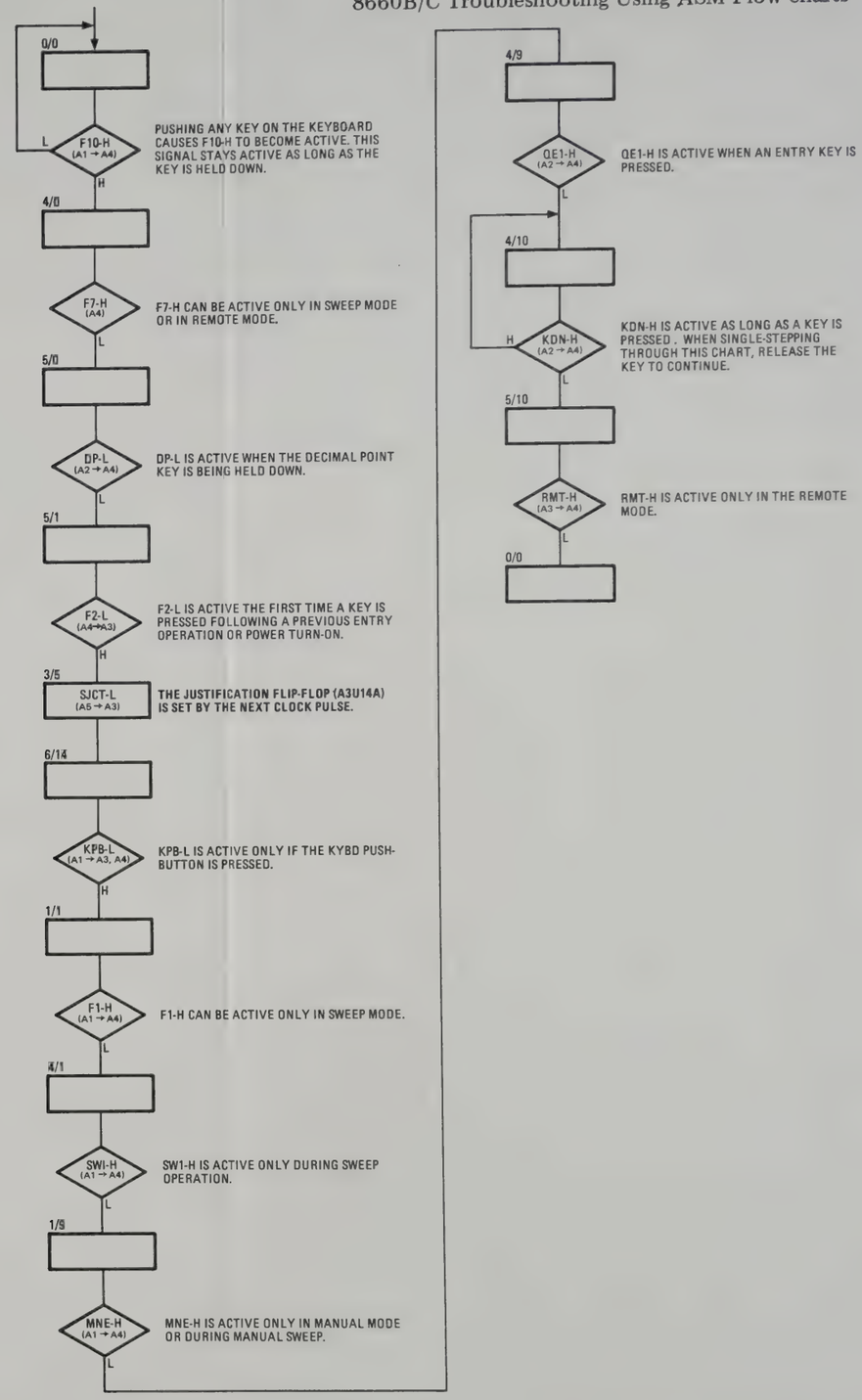


Figure 12-4. ASM Troubleshooting Flow Chart for Decimal Point Key Pressed

UNITS KEY PRE

When a units key (GHz, MHz, kHz, or Hz)
ter is cleared. During state 1/6 the justifica
shifting the data in the keyboard shift regis
the units selected. Justification takes place
circuit description for this assembly in the
justification operation. No other changes
0/0.

HOW

1. Turn the LINE switch to STBY and t
2. Press the "1" key and release.
3. Ground the DCU MAN TP momentar
4. Press one of the UNITS key and hold
5. Single step the ASM using the MAN S

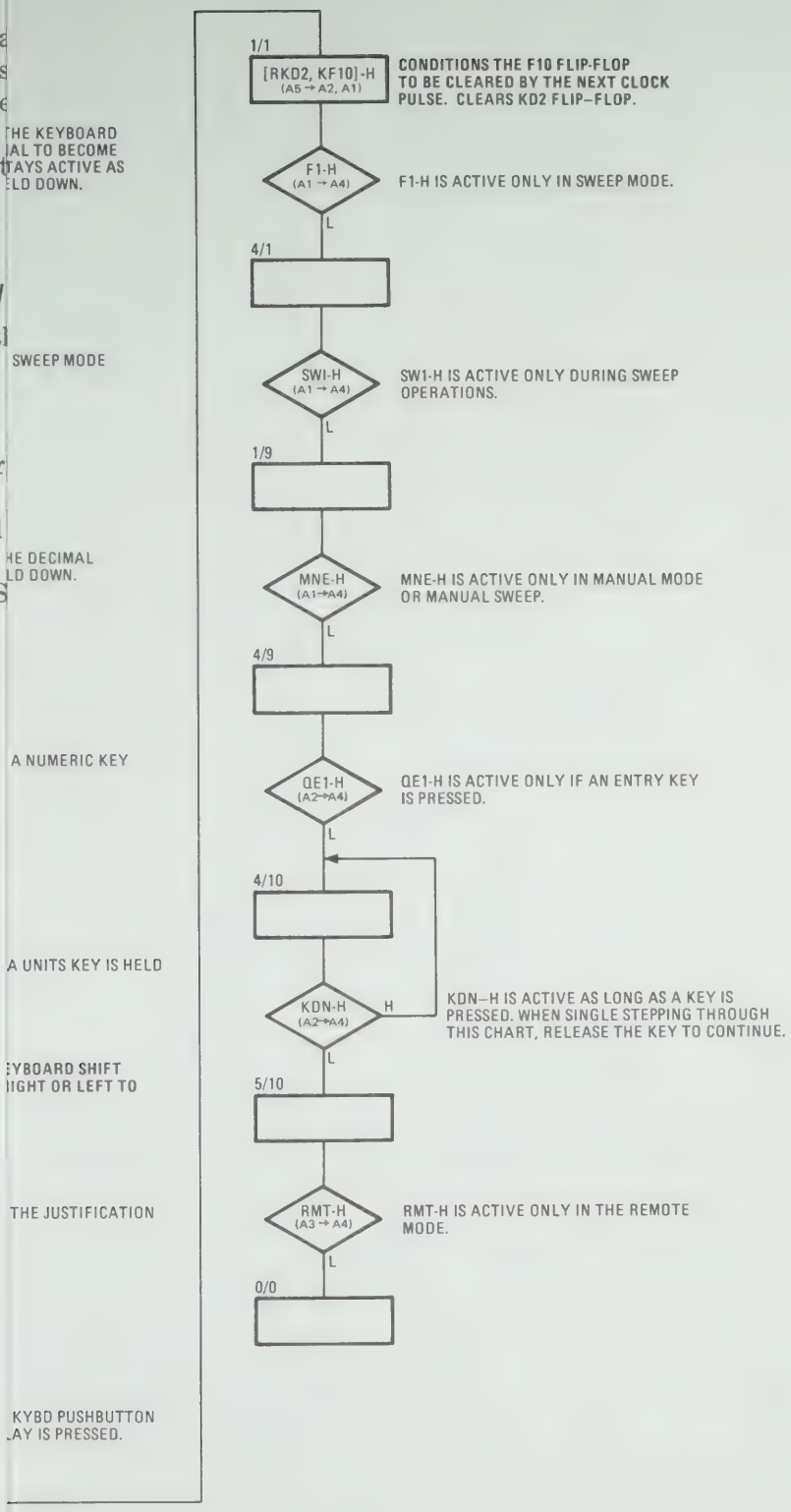


Figure 12-5. ASM Troubleshooting Flow Chart for Units Key Pressed

UNITS KEY PRESSED 0 DATA FLOW

When a units key (GHz, MHz, kHz, or Hz) is pressed, state 0/4 is reached and the K0 register is cleared. During state 1/6 the justification operation takes place. Justification means shifting the data in the keyboard shift register so the decimal point is in the right place for the units selected. Justification takes place on the A3 Readout Control Assembly. The circuit description for this assembly in the 8660 manual contains a good description of the justification operation. No other changes to the data occur and the ASM returns to state 0/0.

HOW TO USE

1. Turn the LINE switch to STBY and then to ON to initialize instrument.
2. Press the "1" key and release.
3. Ground the DCU MAN TP momentarily.
4. Press one of the UNITS key and hold pressed-in.
5. Single step the ASM using the MAN SW and check using the troubleshooting flow chart.

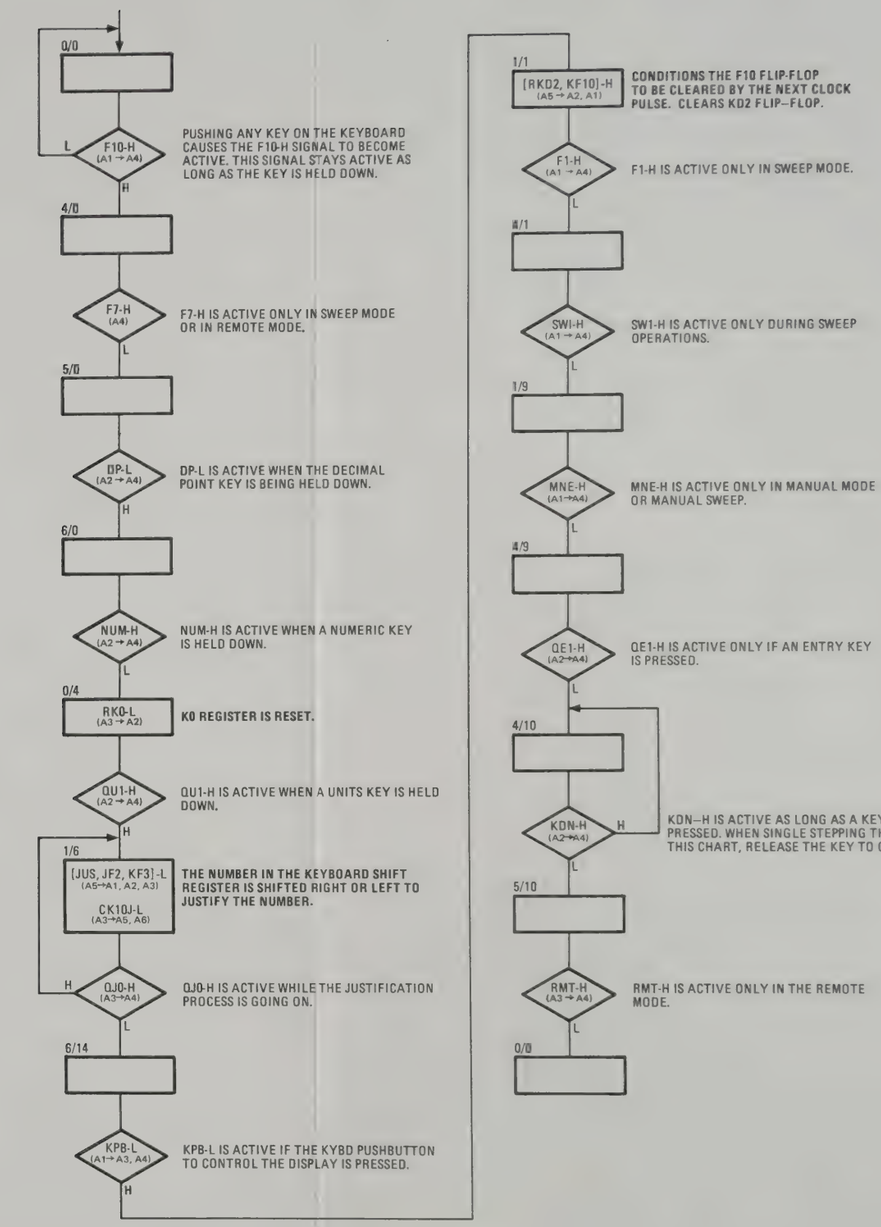


Figure 12-5. ASM Troubleshooting Flow Chart for Units Key Pressed

CF KEY P

Center frequency data is first entered i
keys and a units key. This process is c
After the CF key is pressed and during
Only the six most significant digits app
fer the keyboard shift register still cont
routed back to the input through MPX
limits decoder driven by the M register
frequency is above the upper limit, QA
old center frequency data is put in the
used.

When the frequency is within limits, Q
which data is transferred from the keyb
register. As each digit is placed on the
ultaneously. During state 3/7 data is tr
the Output register. The new data is ser

HC

1. Turn the LINE switch to STBY an
2. Press a series of one or more nume
3. Ground the DCU MAN TP momen
4. Press the CF key and hold pressed
5. Single step the ASM using the MA

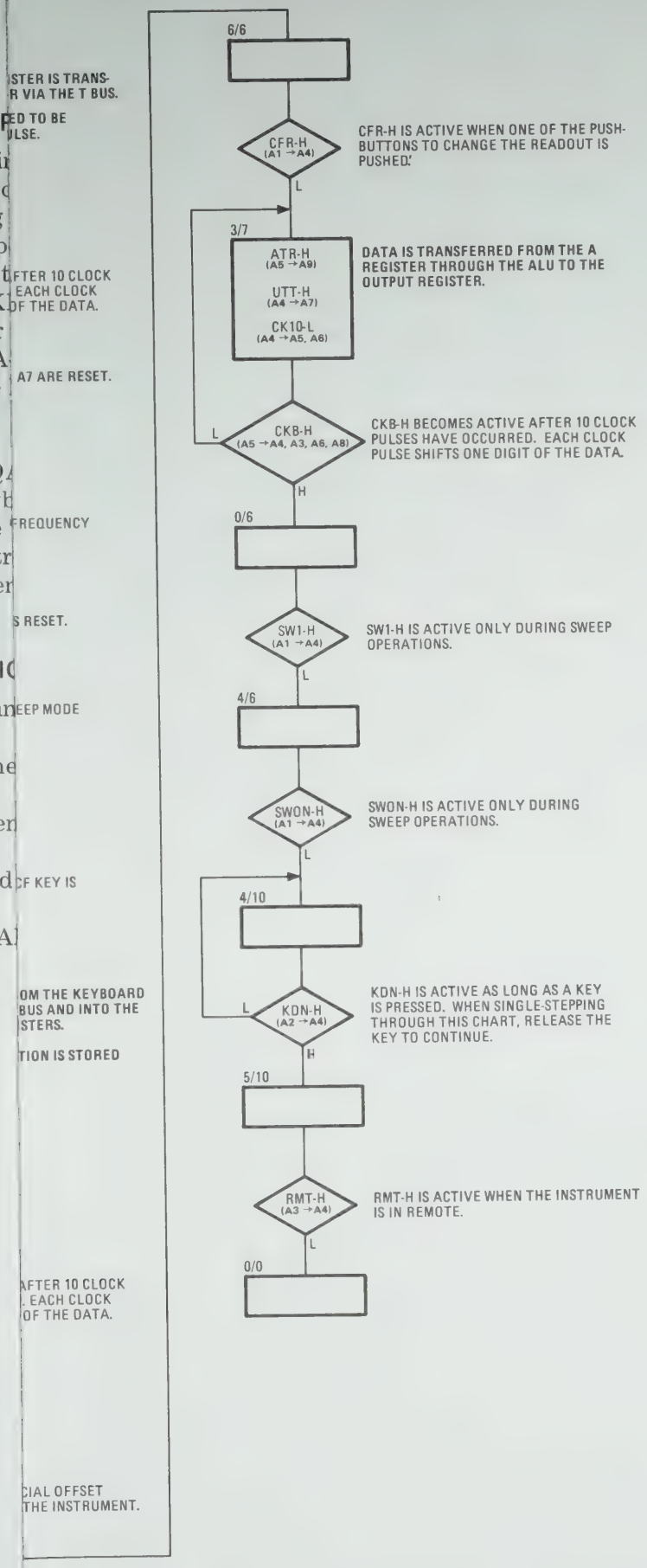


Figure 12-6. ASM Troubleshooting Flow Chart for CF Key Pressed

CF KEY PRESSED DATA FLOW

Center frequency data is first entered into the keyboard shift register by pushing numeric keys and a units key. This process is covered by other charts (Figures 12-3 and 12-5). After the CF key is pressed and during state 1/12 this data is transferred to the M register. Only the six most significant digits appear in the M register. At the end of this data transfer the keyboard shift register still contains the original data because every output digit is routed back to the input through MPXIII (I_1 input) and MPXII (I_2 input). The frequency limits decoder driven by the M register generates the QA-H signal. When the new center frequency is above the upper limit, QA-H becomes active and state 2/3 is entered. The old center frequency data is put in the M register during state 3/8. The new data is not used.

When the frequency is within limits, QA-H is not active and state 2/5 is reached during which data is transferred from the keyboard shift register to the CF, A, and Read Out register. As each digit is placed on the T bus it is clocked into each of these registers simultaneously. During state 3/7 data is transferred from the A register through the ALU to the Output register. The new data is sent to the loops after all 10 digits are in the A register.

HOW TO USE

1. Turn the LINE switch to STBY and then to ON to initialize instrument.
2. Press a series of one or more numeric keys followed by a units key.
3. Ground the DCU MAN TP momentarily.
4. Press the CF key and hold pressed in.
5. Single step the ASM using the MAN SW and check using the troubleshooting flow chart.

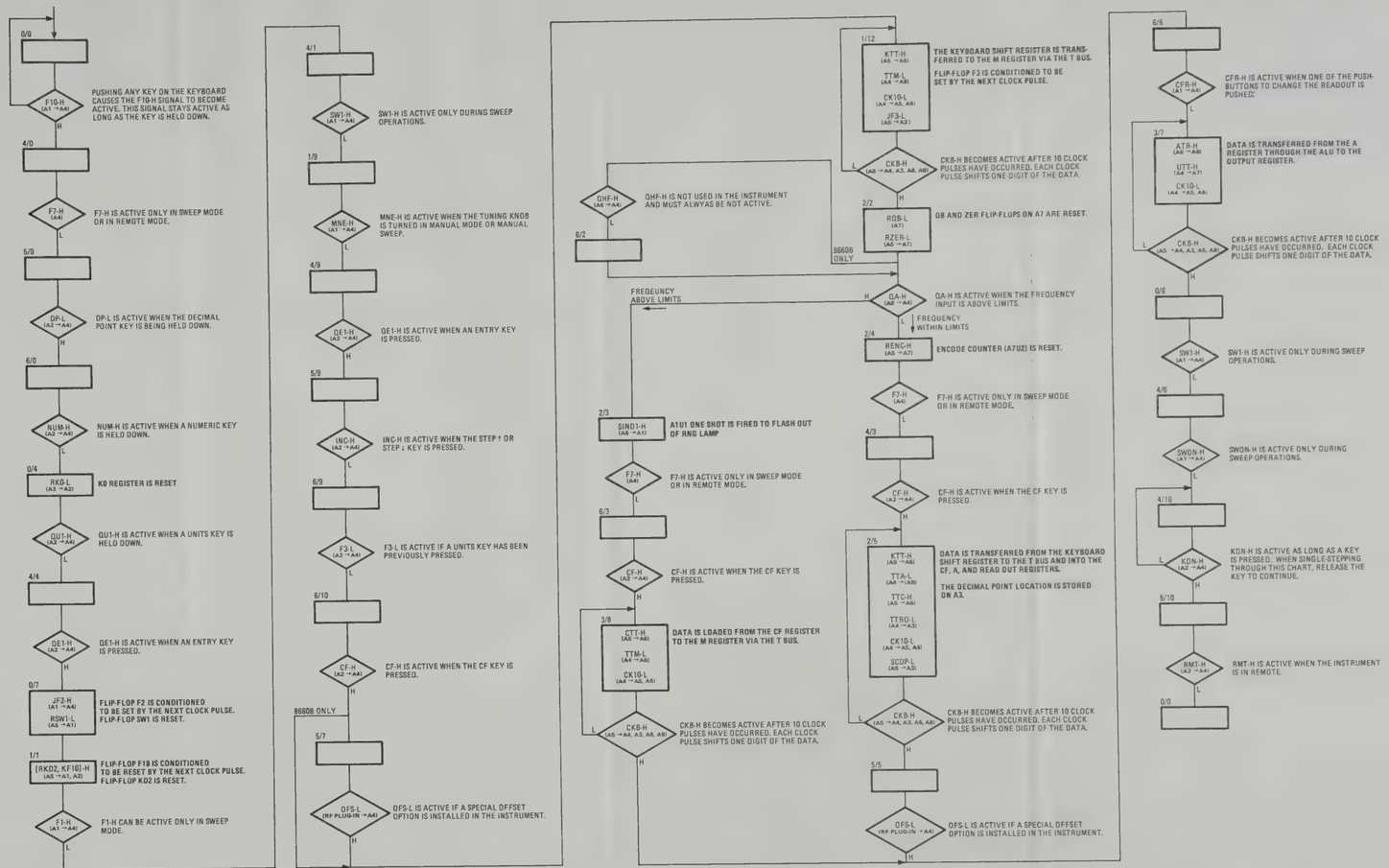


Figure 12-6. ASM Troubleshooting Flow Chart for CF Key Pressed

SWP WIDTH KE

Sweep width data is first entered into th
and a units key. This process is covered
the SWP WIDTH key is pressed and dur
transferred to the Sweep Width Registe
remaining state sequence as explained o

HC

1. Turn the LINE switch to STBY an
2. Press a series of one or more nume
3. Ground the DCU MAN TP momen
4. Press the SWP WIDTH key and ho
5. Single step the ASM using the MA
chart.

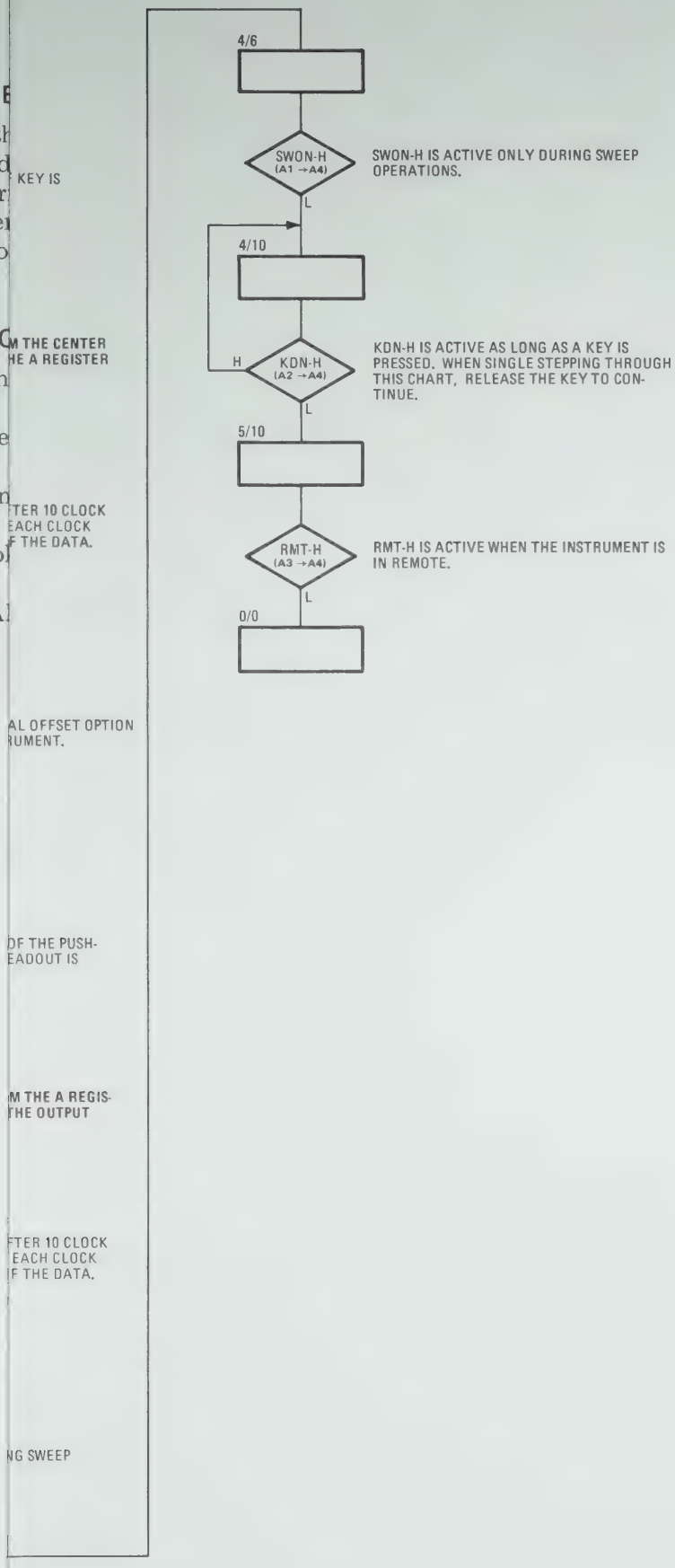


Figure 12-7. ASM Troubleshooting Flow Chart for SWP Width Key Pressed

STEP ↑ AND STEP

If data was entered before the STEP ke
state the data in the Keyboard Register
is bypassed if no data was entered. In t
State 5/13 is entered and the next state
lected. The step up operation will be d

State 1/15 is entered and during this st
Register and the Step Register is added
center frequency data and it is entered
new center frequency is within limits, s
ferred from the CF Register to the A R
frequency is not within limits, state 1/1
Step Register is subtracted from the da
the CF Register and M Register. This s
the value it had before the step was adc

State 3/7 is reached and during this sta
the ALU without modification to the C
put Register, the new data is sent to th

HC

1. Turn the LINE switch to STBY ar
2. Enter 50 MHz Center Frequency
3. Press and release the "1" key and
4. Ground the DCU MAN TP momer
5. Press the STEP↑ or STEP↓ key an
6. Single step the ASM using the MA chart.

FROM THE CENTER
O THE A REGISTER
R VIA THE T BUS.

E AFTER 10 CLOCK
D. EACH CLOCK
T OF THE DATA.

ECIAL OFFSET
N THE INSTRUMENT.

ONE OF THE PUSH-
HE READOUT IS

ROM THE A REGIS-
TO THE OUTPUT

E AFTER 10 CLOCK
D. EACH CLOCK
T OF THE DATA.

URING SWEEP

DURING SWEEP

G AS A KEY IS
STEPPING THROUGH
HE KEY TO CON-

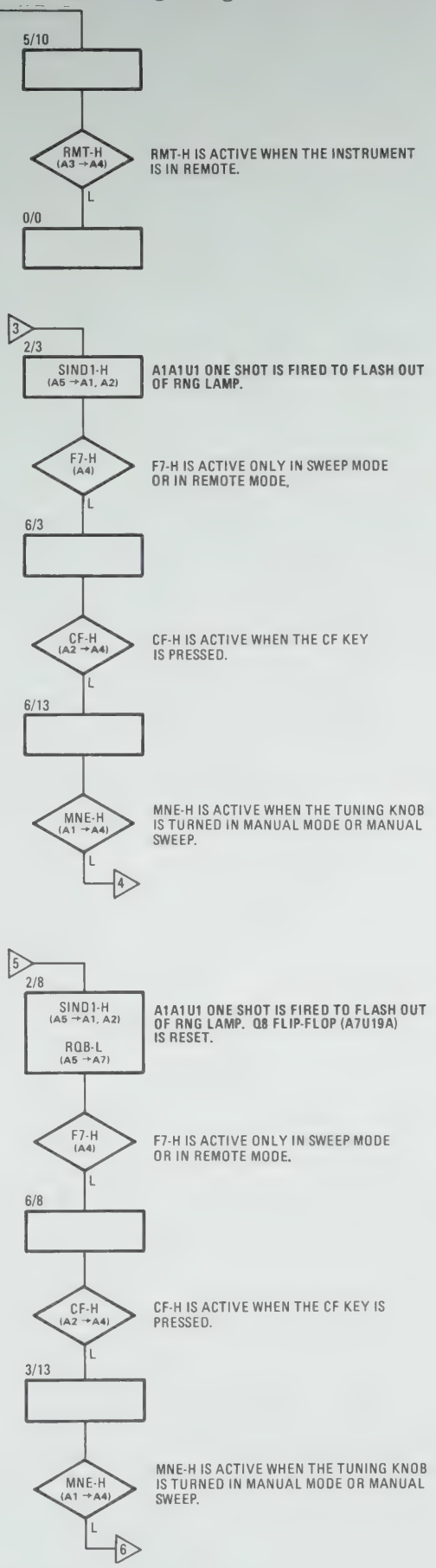


Figure 12-8. ASM Troubleshooting Flow Chart for STEP ↑ or STEP↓ Key Pressed

SWP WIDTH KEY PRESSED DATA FLOW

Sweep width data is first entered into the keyboard shift register by pushing numeric keys and a units key. This process is covered by other charts (Figures 12-3 and 12-5). After the SWP WIDTH key is pressed and during state 1/11 the data in the keyboard register is transferred to the Sweep Width Register. Center frequency data is transferred during the remaining state sequence as explained on the flow chart.

HOW TO USE

1. Turn the LINE switch to STBY and then to ON to initialize the instrument.
2. Press a series of one or more numeric keys followed by a units key.
3. Ground the DCU MAN TP momentarily.
4. Press the SWP WIDTH key and hold pressed in.
5. Single step the ASM using the MAN SW and check using the troubleshooting flow chart.

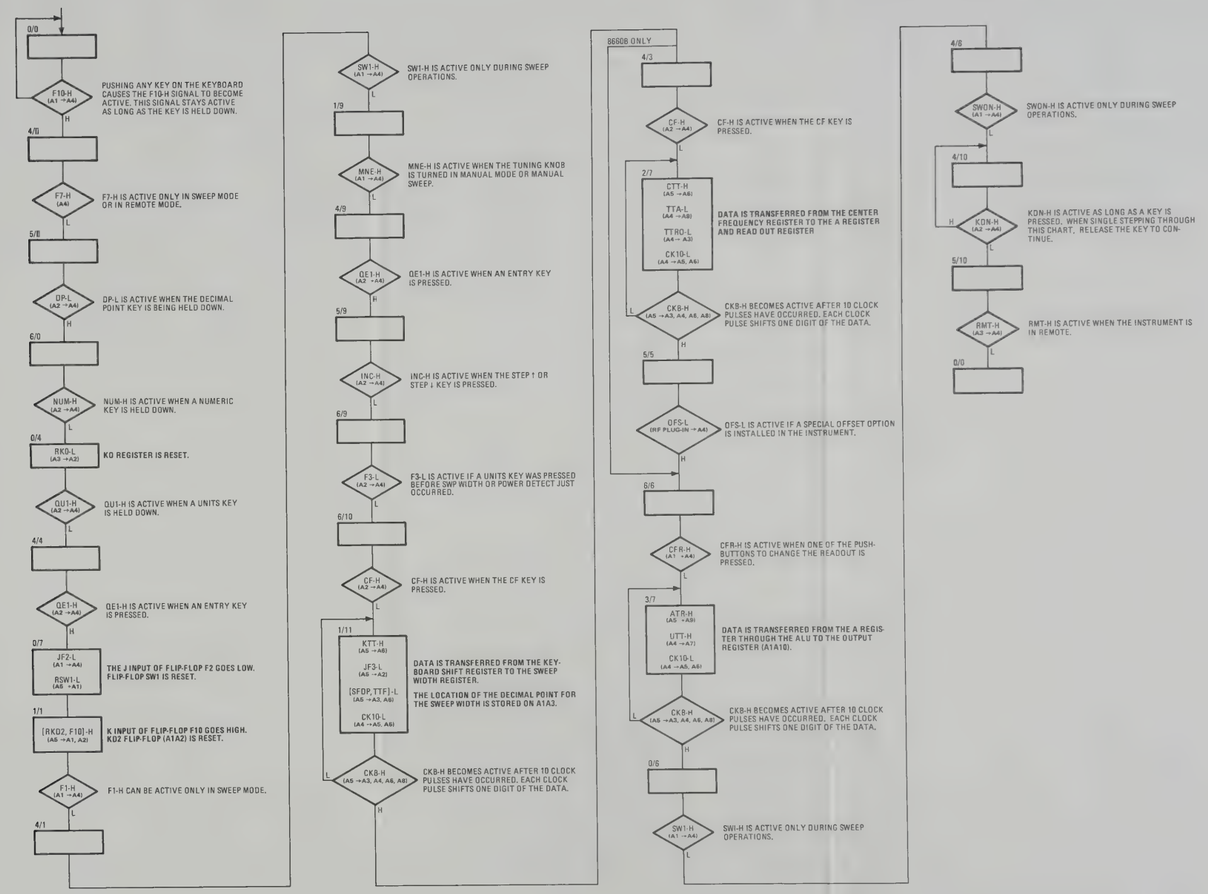


Figure 12-7. ASM Troubleshooting Flow Chart for SWP Width Key Pressed

MANUAL T

When the manual tune knob is turned, t
5/15 where a branch is made. For incre
manual tune increment (from ROM #4
stored in the CF and M Registers. Like
2/0 is reached and the increment is subt
below limits, the increment is subtracte
to its original value.

The ASM then continues to state 2/7 d
Out Registers. When state 3/7 is reache
output register. The ASM then returns

HC

1. Turn the LINE switch to STBY ar
2. Turn the MANUAL MODE RESO
3. Enter 50 MHz center frequency o
4. Ground the DCU MAN TP momer
5. Turn the TUNING knob a small a
6. Press the MAN SW pushbutton an
   chart. When single stepping the A
   by the correct value but the ASM

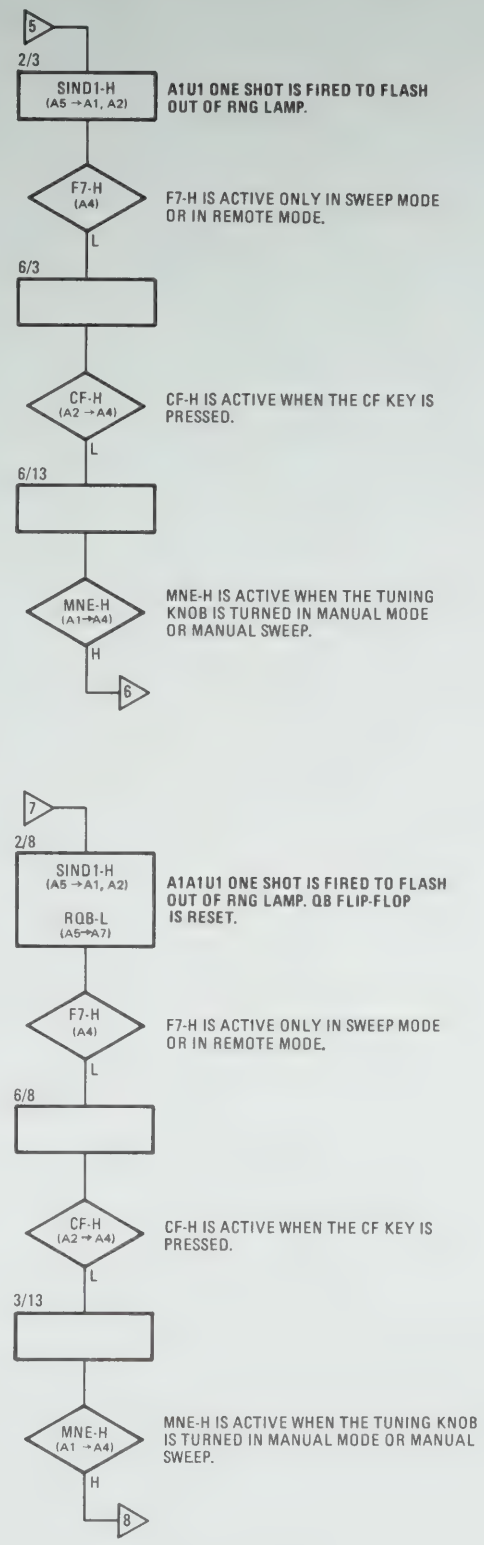


Figure 12-9. ASM Troubleshooting Flow Chart for Manual Tune

STEP ↑ AND STEP ↓ KEY PRESSED DATA FLOW

If data was entered before the STEP key was pressed, state 1/13 is entered. During this state the data in the Keyboard Register is transferrred to the Step Register. State 1/13 is bypassed if no data was entered. In this case the previously entered step size is used. State 5/13 is entered and the next state depends on whether STEP↑ or STEP↓ was selected. The step up operation will be described.

State 1/15 is entered and during this state the data from the Center Frequency (CF) Register and the Step Register is added in the ALU. The output of the ALU is the new center frequency data and it is entered into the M Register and the CF Register. If the new center frequency is within limits, state 2/7 is reached during which the data is transferred from the CF Register to the A Register and Read Out Register. If the new center frequency is not within limits, state 1/14 is entered and during this state the data in the Step Register is subtracted from the data in the CF Register and the result is entered in the CF Register and M Register. This subtraction returns the center frequency data to the value it had before the step was added and produced an out of limits value.

State 3/7 is reached and during this state data is transferred from the A Register through the ALU without modification to the Output Register. When all 10 digits are in the Output Register, the new data is sent to the mainframe loops.

HOW TO USE

1. Turn the LINE switch to STBY and then to ON to initialize the instrument.
2. Enter 50 MHz Center Frequency on the keyboard.
3. Press and release the "1" key and then the "MHz" key.
4. Ground the DCU MAN TP momentarily.
5. Press the STEP↑ or STEP↓ key and hold pressed in.
6. Single step the ASM using the MAN SW and check using the troubleshooting flow chart.

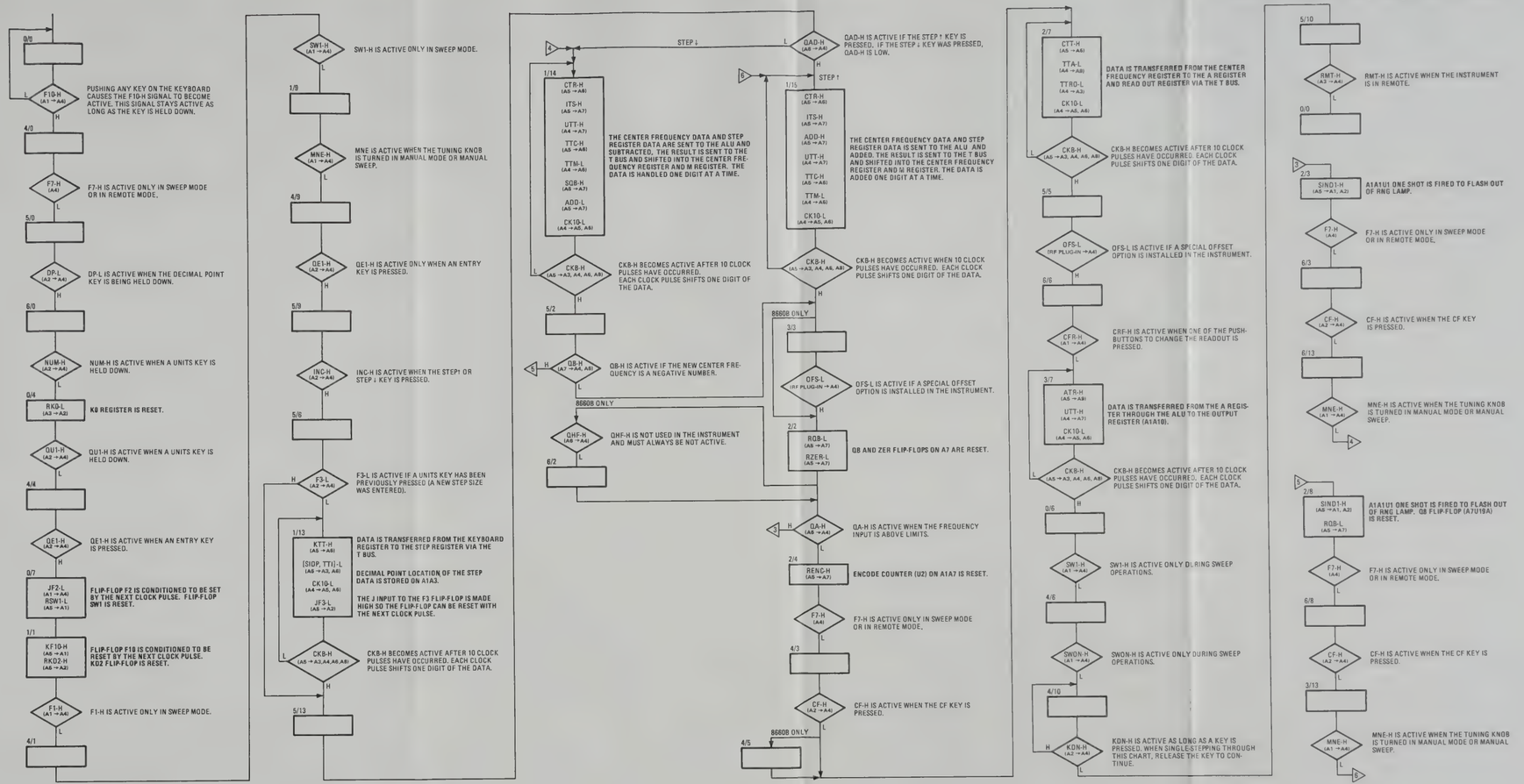


Figure 12-8. ASM Troubleshooting Flow Chart for STEP ↑ or STEP↓ Key Pressed

AUTO S

Turning the SWEEP MODE switch to A
begins the sequence. When state 0/13 i
on A8. At state 0/10 the state machine
checked in state 0/10 is set whenever it
active, state 3/1 or 3/0 is reached durin
by 1/100 or 1/1000 of the value in the
this is accomplished is contained in serv

Something unique happens the first tim
reached, F8-H is not yet active and the
loop between 3/14 and 4/11 until the s
QCTM-H becomes active. Each time th
incremented, but this frequency data is
counter reaches maximum, the A Regis
range. In this condition when state 5/1
to state 2/15 during which the Sweep W
and F8-H is made active. The result wh
placed in the A Register. The ASM the
F8-H is active so state 0/9 is entered du
to the Output Register thus changing th

The ASM now goes into a loop betwee
the A Register is incremented and then
After 1000 times (100 times in FAST F
the upper limit of the sweep range and
enters state 6/11 where the Sweep Widt
the sweep counter is reset. The loop be
sequence continues as long as the SWE

1. Turn the LINE switch to STBY an
2. Enter 50 MHz Center Frequency f
3. Enter 1 MHz Sweep Width from th
4. Ground the DCU MAN TP momer
5. Turn the SWEEP MODE to AUTO
6. Single step the ASM using the MA
   The ASM enters a loop between st
   (50 times with SWEEP MODE in F
   part of the flow chart. There are t

   (1) Use a logic analyzer.

   (2) Put the DCU in AUTO by mo
   onds later return the DCU to
   states 3/14 and 0/9 and you
   check that part of the sequen
   the A Register since this only

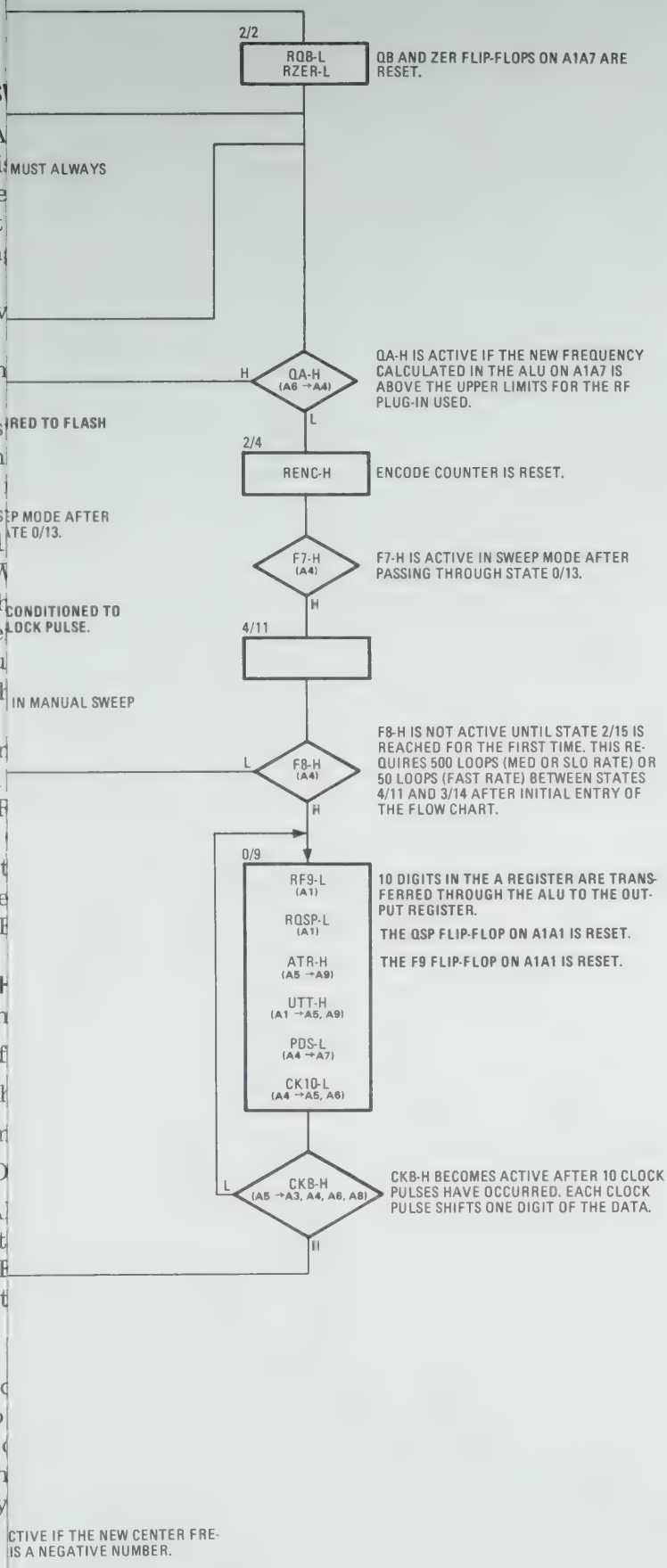


Figure 12-10. ASM Troubleshooting Flow Chart for Auto Sweep

MANUAL TUNE DATA FLOW

When the manual tune knob is turned, the ASM enteres state 4/0 and proceeds to state 5/15 where a branch is made. For increasing frequency state 2/1 is entered and the manual tune increment (from ROM #4 on A7) is added to the center frequency and stored in the CF and M Registers. Likewise if the frequency is to be decreased, state 2/0 is reached and the increment is subtracted. If the new center frequency is above or below limits, the increment is subtracted or added out to return the center frequency to its original value.

The ASM then continues to state 2/7 during which data is transferred to the A and Read-Out Registers. When state 3/7 is reached, data is transferred from the A Register to the output register. The ASM then returns to state 0/0.

HOW TO USE

1. Turn the LINE switch to STBY and then to ON to initialize instrument.
2. Turn the MANUAL MODE RESOLUTION switch to COURSE.
3. Enter 50 MHz center frequency on the keyboard.
4. Ground the DCU MAN TP momentarily.
5. Turn the TUNING knob a small amount.
6. Press the MAN SW pushbutton and check the ASM using the troubleshooting flow chart. When single stepping the ASM, the center frequency doesn't always increment by the correct value but the ASM state sequence functions correctly.

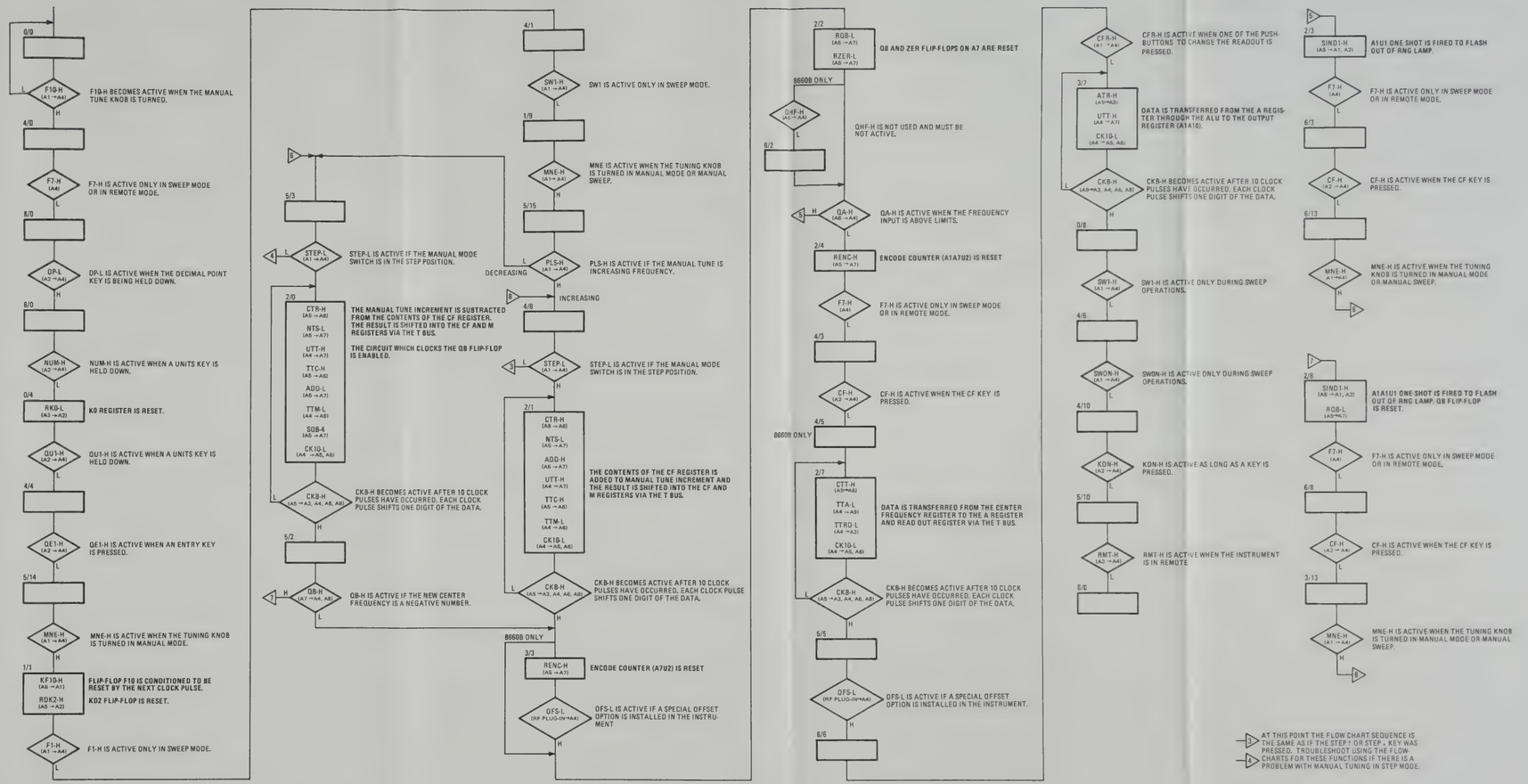


Figure 12-9. ASM Troubleshooting Flow Chart for Manual Tune

KYBD PUSHBU

When the KYBD pushbutton is pressed
data on the Keyboard Shift Register is
The ASM goes to state 0/0 where it rem
leasing the pushbutton allows the ASM
which the data in the Center Frequency

HC

1. Turn the LINE switch to STBY ar
2. Press a series of numeric keys foll
keyboard register.
3. Ground the DCU MAN TP momer
4. Press the KYBD button and hold
5. Single step the ASM using the MA
chart. When state 0/0 is reached,
stepping.

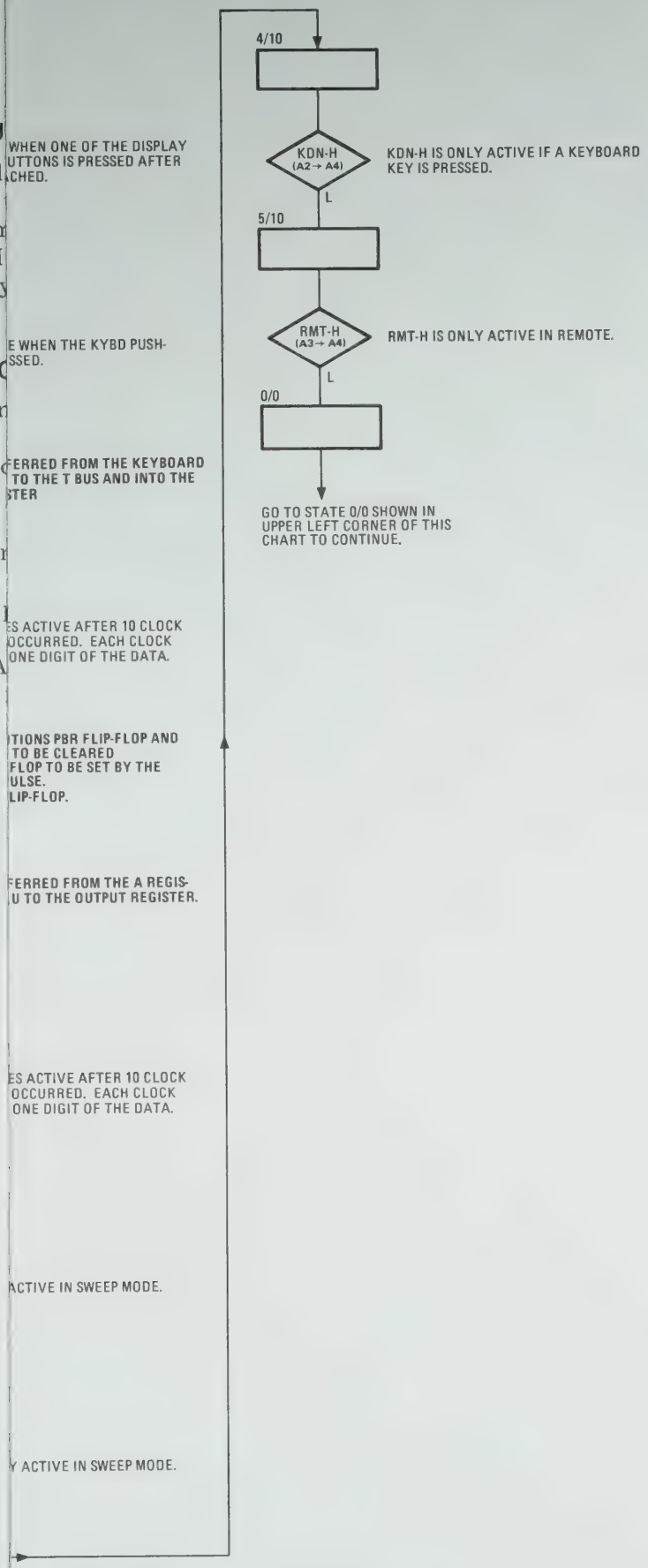


Figure 12-11. ASM Troubleshooting Flow Chart for KYBD Pushbutton Pressed

AUTO SWEEP DATA FLOW

Turning the SWEEP MODE switch to AUTO causes the ASM to move to state 4/0 which begins the sequence. When state 0/13 is reached, 500 is loaded into the sweep counter on A8. At state 0/10 the state machine enters a wait loop. The QSP flip-flop which is checked in state 0/10 is set whenever it is time to step in frequency. After QSP-H becomes active, state 3/1 or 3/0 is reached during which the number in the A register is incremented by 1/100 or 1/1000 of the value in the Sweep Width Register. An explanation of how this is accomplished is contained in service sheet 32 of the 8660C manual.

Something unique happens the first time through the flow chart. When state 4/11 is reached, F8-H is not yet active and the ASM goes to state 3/14. The ASM continues to loop between 3/14 and 4/11 until the sweep counter or A8 reaches a count of 1000 and QCTM-H becomes active. Each time through this loop the frequency in the A register is incremented, but this frequency data is never sent to the Output Register. When the sweep counter reaches maximum, the A Register also contains the upper frequency in the sweep range. In this condition when state 5/11 is reached, the ASM goes to state 6/11 and then to state 2/15 during which the Sweep Width Register is subtracted from the A Register and F8-H is made active. The result which is the lowest frequency in the sweep range is placed in the A Register. The ASM then goes to state 2/2 and when state 4/11 is reached, F8-H is active so state 0/9 is entered during which the data in the A Register is transferred to the Output Register thus changing the output frequency.

The ASM now goes into a loop between states 3/14 and 0/9. Each time through the loop the A Register is incremented and then the new value is transferred to the Output Register. After 1000 times (100 times in FAST RATE) through the loop the output frequency is at the upper limit of the sweep range and QCTM-H becomes active again. The ASM then enters state 6/11 where the Sweep Width Register is subtracted from the A Register and the sweep counter is reset. The loop between states 3/14 and 0/9 is entered again. This sequence continues as long as the SWEEP MODE is set to AUTO.

HOW TO USE

1. Turn the LINE switch to STBY and then to ON to initialize the instrument.
2. Enter 50 MHz Center Frequency from the keyboard.
3. Enter 1 MHz Sweep Width from the keyboard.
4. Ground the DCU MAN TP momentarily.
5. Turn the SWEEP MODE to AUTO and the RATE to MED.
6. Single step the ASM using the MAN SW and check using the troubleshooting flow chart. The ASM enters a loop between states 3/14 and 4/11 which it passes through 500 times. (50 times with SWEEP MODE in FAST). This makes single stepping unusable for this part of the flow chart. There are two things which can be done:
   (1) Use a logic analyzer.
   (2) Put the DCU in AUTO by momentarily grounding the AUTO TP. Then a few seconds later return the DCU to manual. The ASM should now be in the loop between states 3/14 and 0/9 and you can check this loop. It's very difficult to manually check that part of the sequence where the Sweep Width Register is subtracted from the A Register since this only happens once for every 1000 times through the loop.

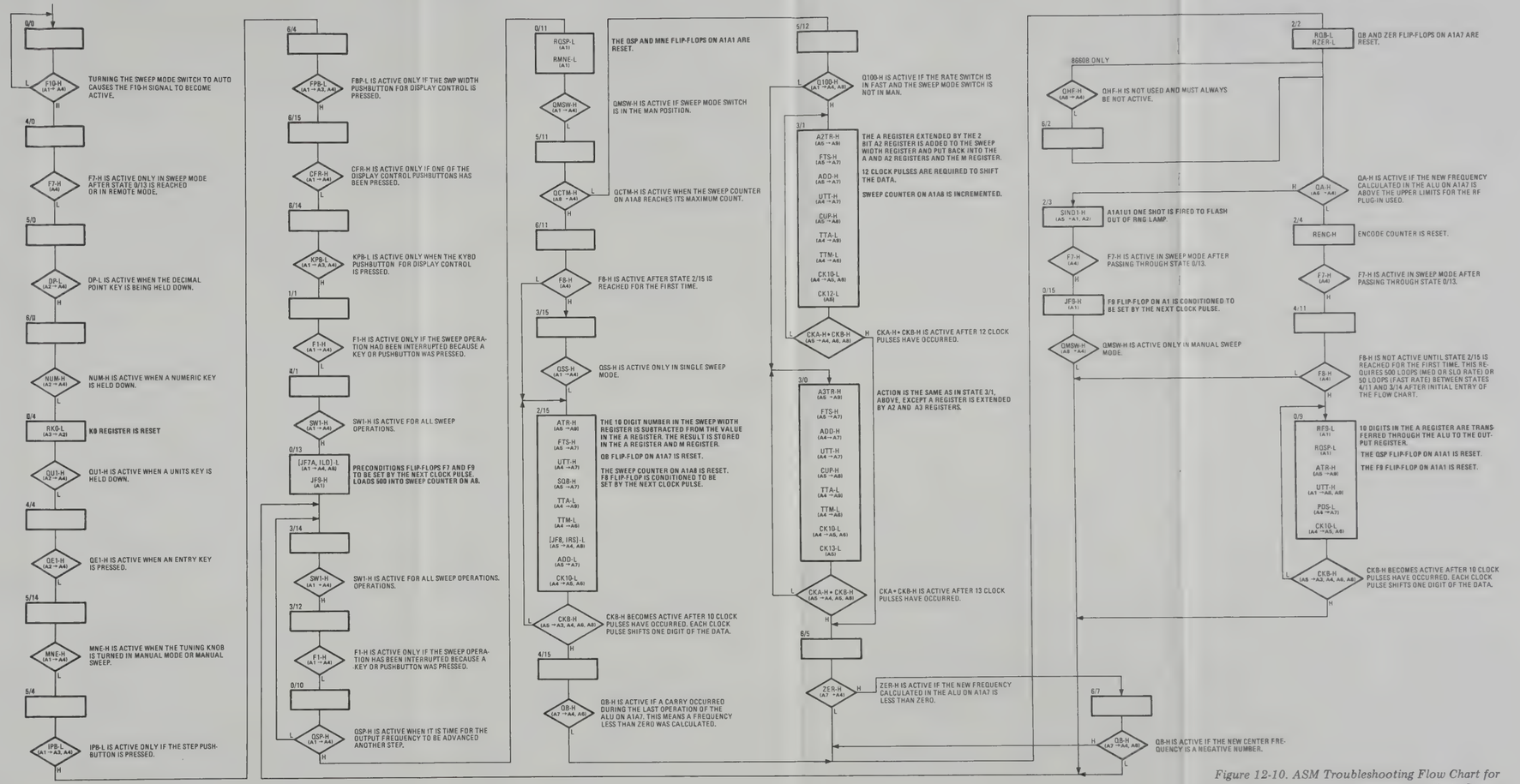


Figure 12-10. ASM Troubleshooting Flow Chart for Auto Sweep

POWER-ON IN

When the power detect signal from the A
on sequence. During state 1/6 MHz is st
reached, the CF Register (which was clea
from ROM #4 on the ALU board and th
state 2/7 the data in the CF Register is t
when state 3/7 is reached, data is transfe

1. Turn the LINE switch to STBY.
2. Connect a test lead from ground
3. Turn the LINE switch to ON.
4. Single step the ASM using the M
chart.

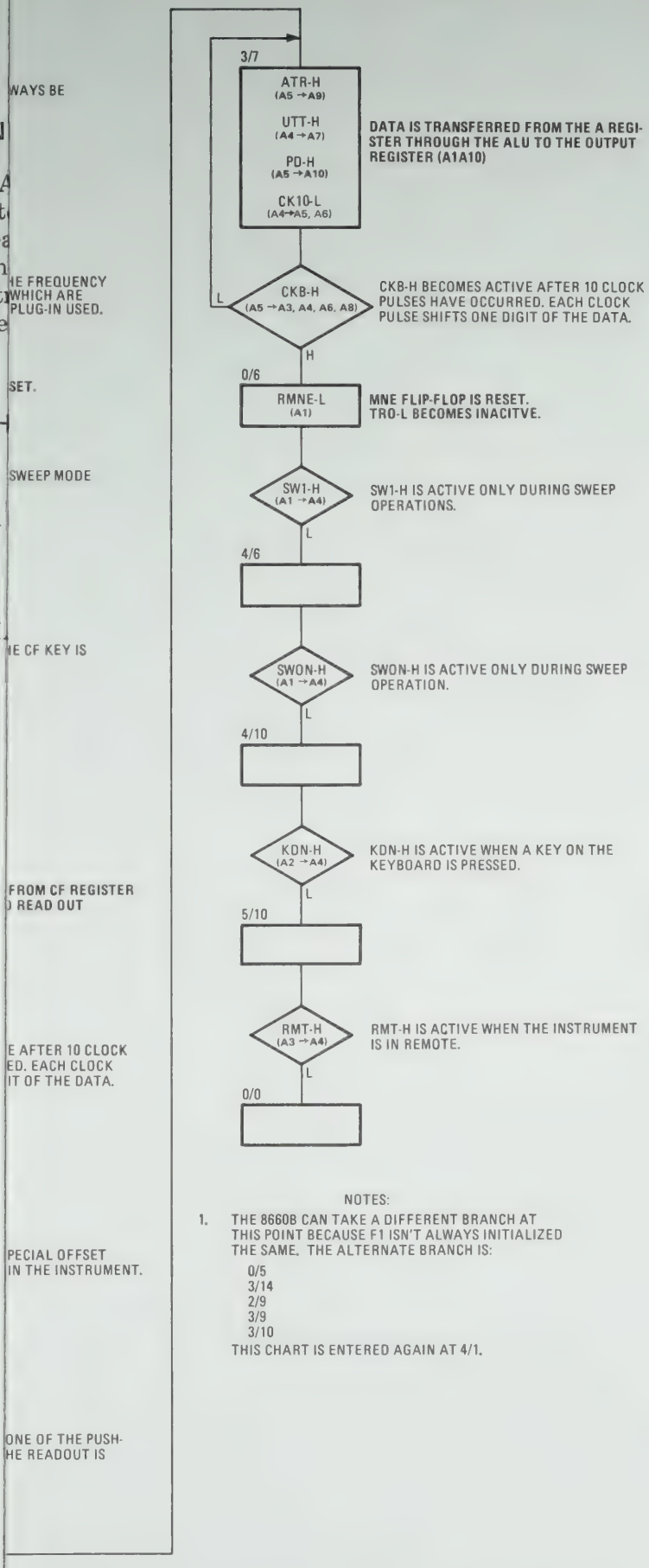


Figure 12-12. ASM Troubleshooting Flow Chart for Power-On Initialization

KYBD PUSHBUTTON PRESSED DATA FLOW

When the KYBD pushbutton is pressed, state 4/0 is entered. When state 1/4 is reached, the data on the Keyboard Shift Register is transferred via the T bus to the Read Out Register. The ASM goes to state 0/0 where it remains until the KYBD pushbutton is released. Releasing the pushbutton allows the ASM to leave state 0/0 and continue to state 1/8 during which the data in the Center Frequency Register is transferred to the Read Out Register.

HOW TO USE

1. Turn the LINE switch to STBY and then to ON to initialize the instrument.
2. Press a series of numeric keys followed by a units key. This places an entry in the keyboard register.
3. Ground the DCU MAN TP momentarily.
4. Press the KYBD button and hold pressed in.
5. Single step the ASM using the MAN SW and check using the troubleshooting flow chart. When state 0/0 is reached, release the KYBD button and continue single stepping.

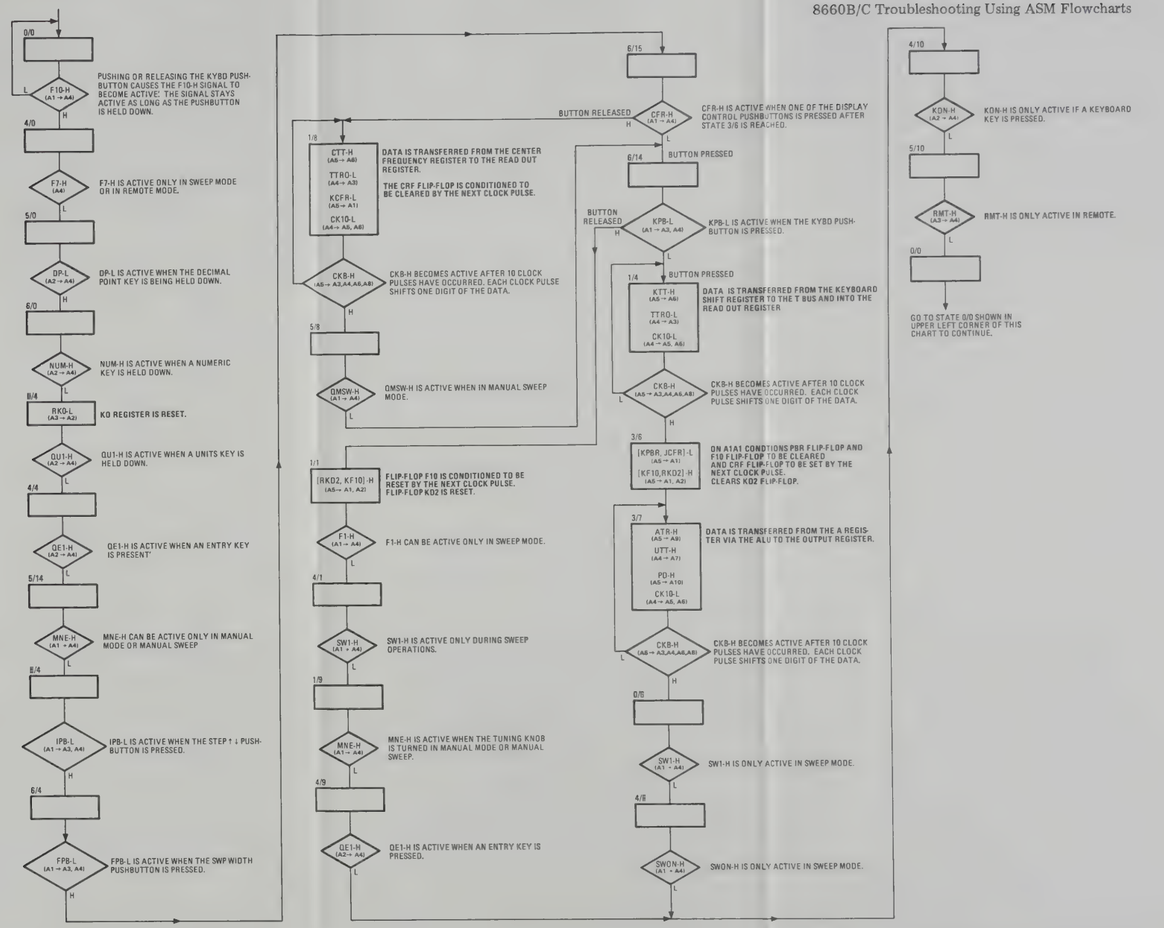


Figure 12-11. ASM Troubleshooting Flow Chart for KYBD Pushbutton Pressed

APPENDIX A
TABLES OF CENTER FREQUENCY VERSUS LOOP FREQUENCIES

Note: these tables do not contain all possible frequency combinations.

Table A-1. Mainframe High Frequency Loop

Programmed Frequency	High Frequency Loop Frequency
000 MHz	450 MHz
010 MHz	440 MHz
020 MHz	430 MHz
030 MHz	420 MHz
040 MHz	410 MHz
050 MHz	400 MHz
060 MHz	390 MHz
070 MHz	380 MHz
080 MHz	370 MHz
090 MHz	360 MHz
100 MHz	*350 MHz
*450 MHz if 86602A is installed.	

$$f_{HF} = 450 - (D_8 \times 10) \text{ MHz}$$

Table A-2. Mainframe N1 Loop Frequencies

Programmed Frequency	N1 Frequency
0.0 MHz	29.7 MHz
0.1 MHz	29.6 MHz
0.2 MHz	29.5 MHz
0.3 MHz	29.4 MHz
0.4 MHz	29.3 MHz
0.5 MHz	29.2 MHz
0.6 MHz	29.1 MHz
0.7 MHz	29.0 MHz
0.8 MHz	28.9 MHz
0.9 MHz	28.8 MHz
1.0 MHz	28.7 MHz
2.0 MHz	27.7 MHz
3.0 MHz	26.7 MHz
4.0 MHz	25.7 MHz
5.0 MHz	24.7 MHz
6.0 MHz	23.7 MHz
2.0 MHz	22.7 MHz
8.0 MHz	21.7 MHz
9.0 MHz	20.7 MHz
9.1 MHz	20.6 MHz
9.2 MHz	20.5 MHz
9.3 MHz	20.4 MHz
9.4 MHz	20.3 MHz
9.5 MHz	20.2 MHz
9.6 MHz	20.1 MHz
9.7 MHz	20.0 MHz
9.8 MHz	19.9 MHz
9.9 MHz	19.8 MHz

$$f_{N1} = (29.7 - D_7 \cdot D_6) \text{ MHz}$$

Table A-3. Mainframe N2 Loop Frequencies

Programmed Frequency	N2 Frequency
X.X000 MHz	29.79 MHz
X.X001 MHz	29.78 MHz
X.X002 MHz	29.77 MHz
X.X003 MHz	29.76 MHz
X.X004 MHz	29.75 MHz
X.X005 MHz	29.74 MHz
X.X006 MHz	29.73 MHz
X.X007 MHz	29.72 MHz
X.X008 MHz	29.71 MHz
X.X009 MHz	29.70 MHz
X.X010 MHz	29.69 MHz
X.X020 MHz	29.59 MHz
X.X030 MHz	29.49 MHz
X.X040 MHz	29.39 MHz
X.X050 MHz	29.29 MHz
X.X060 MHz	29.19 MHz
X.X070 MHz	29.09 MHz
X.X080 MHz	28.99 MHz
X.X090 MHz	28.89 MHz
X.X100 MHz	28.79 MHz
X.X200 MHz	27.79 MHz
X.X300 MHz	26.79 MHz
X.X400 MHz	25.79 MHz
X.X500 MHz	24.79 MHz
X.X600 MHz	23.79 MHz
X.X700 MHz	22.79 MHz
X.X800 MHz	21.79 MHz
X.X900 MHz	20.79 MHz
X.X999 MHz	19.80 MHz

$$f_{N2} = [29.79 - (D_5 \cdot D_4\, D_3)] \text{ MHz}$$

Table A-4. Mainframe N3 Loop Frequencies

Programmed Frequency	N3 Frequency
X.XXXX00 MHz	2.100 MHz
X.XXXX01 MHz	2.099 MHz
X.XXXX02 MHz	2.098 MHz
X.XXXX03 MHz	2.097 MHz
X.XXXX04 MHz	2.096 MHz
X.XXXX05 MHz	2.095 MHz
X.XXXX06 MHz	2.094 MHz
X.XXXX07 MHz	2.093 MHz
X.XXXX08 MHz	2.092 MHz
X.XXXX09 MHz	2.091 MHz
X.XXXX10 MHz	2.090 MHz
X.XXXX20 MHz	2.080 MHz
X.XXXX30 MHz	2.070 MHz
X.XXXX40 MHz	2.060 MHz
X.XXXX50 MHz	2.050 MHz
X.XXXX60 MHz	2.040 MHz
X.XXXX70 MHz	2.030 MHz
X.XXXX80 MHz	2.020 MHz
X.XXXX90 MHz	2.010 MHz
X.XXXX99 MHz	2.001 MHz

$$f_{N3} = [2.1 - .0D_2\, D_1] \text{ MHz}$$

These tables do not contain all possible frequency combinations.

Table A-5. Mainframe Sum Loop 2 Frequencies

Programmed Frequency	SL2 Frequency	Programmed Frequency	SL2 Frequency
X.X00000 MHz	30.0 MHz	X.X00600 MHz	29.9400 MHz
X.X00001 MHz	29.9999 MHz	X.X00700 MHz	29.9300 MHz
X.X00002 MHz	29.9998 MHz	X.X00800 MHz	29.9200 MHz
X.X00003 MHz	29.9997 MHz	X.X00900 MHz	29.9100 MHz
X.X00004 MHz	29.9996 MHz	X.X01000 MHz	29.9000 MHz
X.X00005 MHz	29.9995 MHz	X.X02000 MHz	29.8000 MHz
X.X00006 MHz	29.9994 MHz	X.X03000 MHz	29.7000 MHz
X.X00007 MHz	29.9993 MHz	X.X04000 MHz	29.6000 MHz
X.X00008 MHz	29.9992 MHz	X.X05000 MHz	29.5000 MHz
X.X00009 MHz	29.9991 MHz	X.X06000 MHz	29.4000 MHz
X.X00010 MHz	29.9990 MHz	X.X07000 MHz	29.3000 MHz
X.X00020 MHz	29.9980 MHz	X.X08000 MHz	29.2000 MHz
X.X00030 MHz	29.9970 MHz	X.X09000 MHz	29.1000 MHz
X.X00040 MHz	29.9960 MHz	X.X10000 MHz	29.0000 MHz
X.X00050 MHz	29.9950 MHz	X.X20000 MHz	28.0000 MHz
X.X00060 MHz	29.9940 MHz	X.X30000 MHz	27.0000 MHz
X.X00070 MHz	29.9930 MHz	X.X40000 MHz	26.0000 MHz
X.X00080 MHz	19.9920 MHz	X.X50000 MHz	25.0000 MHz
X.X00090 MHz	29.9910 MHz	X.X60000 MHz	24.0000 MHz
X.X00100 MHz	29.9900 MHz	X.X70000 MHz	23.0000 MHz
X.X00200 MHz	29.9800 MHz	X.X80000 MHz	22.0000 MHz
X.X00300 MHz	29.9700 MHz	X.X90000 MHz	21.0000 MHz
X.X00400 MHz	29.9600 MHz	X.X99999 MHz	20.0001 MHz
X.X00500 MHz	29.9500 MHz		

$$f_{SL2} = (N2 + \frac{N3}{100})\ \text{MHz} = 30 - D_5 \cdot D_4D_3D_2D_1\ \text{MHz}$$

This table does not contain all possible frequency combinations.

Table A-6. Mainframe Sum Loop 1 Frequencies

Programmed Frequency	SL1 Frequency	Programmed Frequency	SL1 Frequency
0.000000 MHz	30.000000 MHz	0.006000 MHz	29.994000 MHz
0.000001 MHz	29.999999 MHz	0.007000 MHz	29.993000 MHz
0.000002 MHz	29.999998 MHz	0.008000 MHz	19.992000 MHz
0.000003 MHz	29.999997 MHz	0.009000 MHz	29.991000 MHz
0.000004 MHz	29.999996 MHz	0.010000 MHz	29.990000 MHz
0.000005 MHz	29.999995 MHz	0.020000 MHz	29.980000 MHz
0.000006 MHz	29.999994 MHz	0.030000 MHz	29.970000 MHz
0.000007 MHz	29.999993 MHz	0.040000 MHz	29.960000 MHz
0.000008 MHz	29.999992 MHz	0.050000 MHz	29.950000 MHz
0.000009 MHz	29.999991 MHz	0.060000 MHz	29.940000 MHz
0.000010 MHz	29.999990 MHz	0.070000 MHz	29.930000 MHz
0.000020 MHz	29.999980 MHz	0.080000 MHz	29.920000 MHz
0.000030 MHz	29.999970 MHz	0.090000 MHz	29.910000 MHz
0.000040 MHz	29.999960 MHz	0.100000 MHz	29.900000 MHz
0.000050 MHz	29.999950 MHz	0.200000 MHz	29.800000 MHz
0.000060 MHz	29.999940 MHz	0.300000 MHz	29.700000 MHz
0.000070 MHz	29.999930 MHz	0.400000 MHz	29.600000 MHz
0.000080 MHz	29.999920 MHz	0.500000 MHz	29.500000 MHz
0.000090 MHz	29.999910 MHz	0.600000 MHz	29.400000 MHz
0.000100 MHz	29.999900 MHz	0.700000 MHz	29.300000 MHz
0.000200 MHz	29.999800 MHz	0.800000 MHz	29.200000 MHz
0.000300 MHz	29.999700 MHz	0.900000 MHz	29.100000 MHz
0.000400 MHz	29.999600 MHz	1.000000 MHz	29.000000 MHz
0.000500 MHz	29.999500 MHz	2.000000 MHz	28.000000 MHz
0.000600 MHz	29.999400 MHz	3.000000 MHz	27.000000 MHz
0.000700 MHz	29.999300 MHz	4.000000 MHz	26.000000 MHz
0.000800 MHz	29.999200 MHz	5.000000 MHz	25.000000 MHz
0.000900 MHz	29.999100 MHz	6.000000 MHz	24.000000 MHz
0.001000 MHz	29.999000 MHz	7.000000 MHz	23.000000 MHz
0.002000 MHz	29.998000 MHz	8.000000 MHz	22.000000 MHz
0.003000 MHz	29.997000 MHz	9.000000 MHz	21.000000 MHz
0.004000 MHz	29.996000 MHz	9.999999 MHz	20.000001 MHz
0.005000 MHz	29.995000 MHz		

$$f_{SL1} = (N1 + \frac{SL2}{100}) \text{ MHz} = 30 - D_7 \cdot D_6D_5D_4D_3D_2D_1 \text{ MHz}$$

This table does not contain all possible frequency combinations.

Table A-7. Extension Module YIG Loop Frequencies

Programmed Centered Frequency	YIG Loop † Frequency
0 MHz	3.95 GHz ± 0.005 GHz
100 MHz	3.85 GHz ± 0.005 GHz
200 MHz	3.75 GHz ± 0.005 GHz
300 MHz	3.65 GHz ± 0.005 GHz
400 MHz	3.55 GHz ± 0.005 GHz
500 MHz	3.45 GHz ± 0.005 GHz
600 MHz	3.35 GHz ± 0.005 GHz
700 MHz	3.25 GHz ± 0.005 GHz
800 MHz	3.15 GHz ± 0.005 GHz
900 MHz	3.05 GHz ± 0.005 GHz
1000 MHz	2.95 GHz ± 0.005 GHz
1100 MHz	2.85 GHz ± 0.005 GHz
1200 MHz	2.75 GHz ± 0.005 GHz

† The frequency tolerance occurs because of drift in the free-running 4.43 GHz oscillator which is mixed with the YIG Loop output and Sum Loop output. Because the frequency tolerance and drift are identical in both outputs, they cancel when the YIG and SUM frequencies are mixed in the RF Section.

$$f_{YIG} = 3950 - (D_{10}D_9 \times 100)\ \text{MHz}$$

Table A-8. Extension Module SUM Loop Frequencies

Programmed Centered Frequency	11661 SUM Loop *† Frequency
0 MHz	3.950 GHz ± 0.005 GHz
10 MHz	3.960 GHz ± 0.005 GHz
20 MHz	3.970 GHz ± 0.005 GHz
30 MHz	3.980 GHz ± 0.005 GHz
40 MHz	3.990 GHz ± 0.005 GHz
50 MHz	4.000 GHz ± 0.005 GHz
60 MHz	4.010 GHz ± 0.005 GHz
70 MHz	4.020 GHz ± 0.005 GHz
80 MHz	4.030 GHz ± 0.005 GHz
90 MHz	4.040 GHz ± 0.005 GHz
99.999 999	4.049 99 999 ± 0.005 GHz

*The 11661 Sum loop is programmed in 1 Hertz steps by changes in the mainframe SL1 loop frequency. This table checks only the 10 MHz steps since the SL1 output has previously been shown to be good.

† The frequency tolerance occurs because of drift in the free-running 4.43 GHz oscillator which is mixed with the YIG Loop output and Sum Loop output. Because the frequency tolerance and drift are identical in both outputs, they cancel when the YIG and SUM frequencies are mixed in the RF Section.

These tables do not contain all possible frequency combinations.

APPENDIX B
BRIEF THEORY OF OPERATION

The 8660 Synthesized Signal Generator is a phase lock system in which all output frequencies are derived from a single 10 MHz reference oscillator. This technique used to generate the output frequency is called indirect synthesis. In the simplest form of indirect synthesis an oscillator at the desired output frequency is phase locked to the reference oscillator.

In the 8660 a 100 MHz oscillator (on the A4A4 assembly) is phase locked to a 10 MHz crystal controlled reference oscillator. This 100 MHz signal is multiplied to 500 MHz and divided to 20 MHz, 10 MHz, 2 MHz, 400 kHz and 100 kHz. These signals (except for the 2 MHz) are the reference frequencies used to control the mainframe phase lock loops. The 2 MHz signal is used as the clock pulse in the Mainframe digital Control Unit (DCU).

The Mainframe phase lock loop outputs are combined to produce the desired center frequency.

Figure B-1 shows the Block diagram of the 8660 Reference Section.

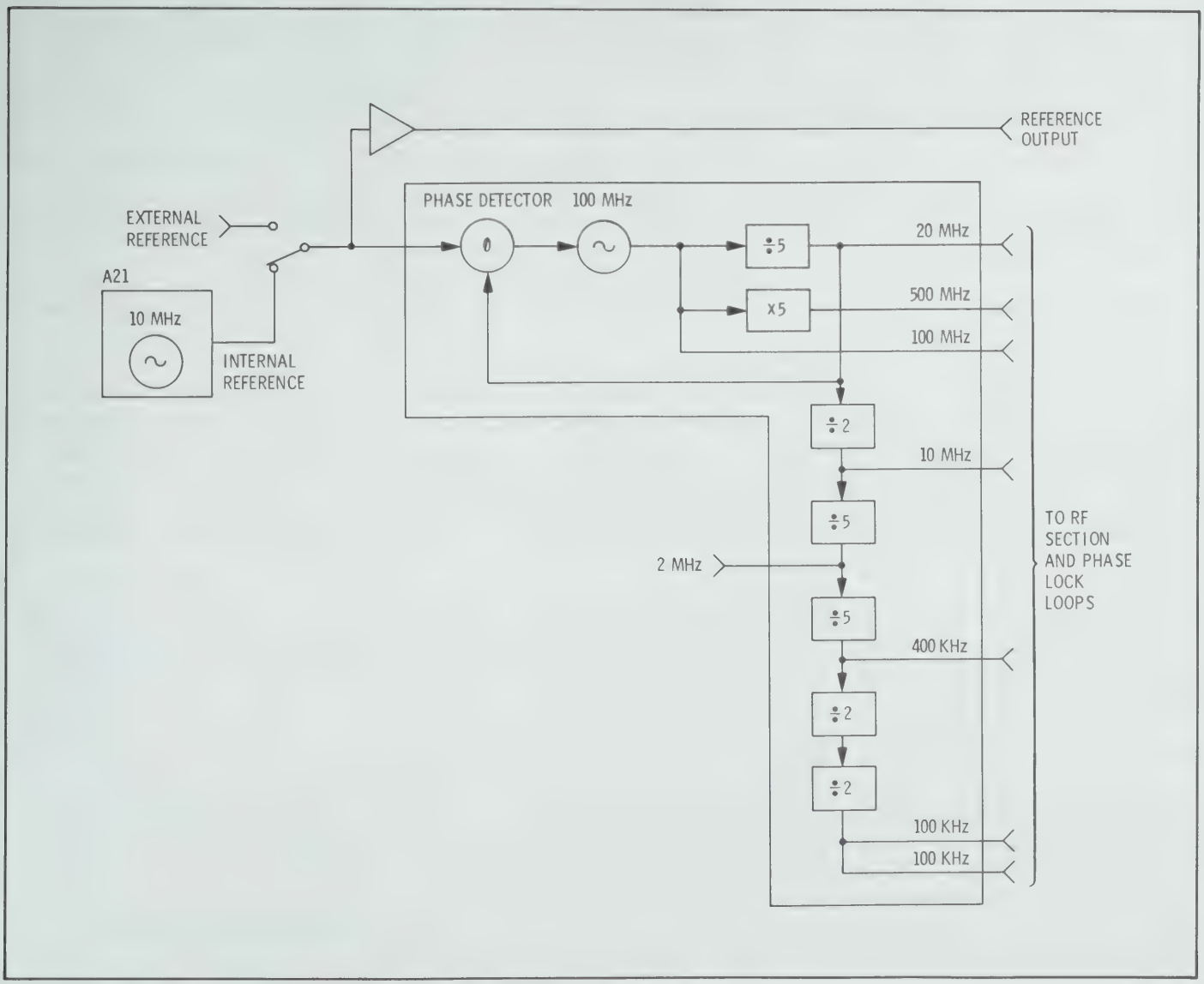


Figure B-1. 8660 Reference Section

All the frequencies generated by the reference section are *fixed* at specific frequencies. To make a useful signal generator, we need an output that is tunable. In the 8660 we meet this requirement with a group of tunable phase lock loops each of which is locked to the 10 MHz reference oscillator by way of the oscillator and dividers in the A4 reference section.

The tunable phase lock loops are shown in Table B-1 along with their exact frequency ranges and the digits in the final output frequency they control.

Digit 1 is the least significant digit (1 Hz digit) and Digit 9 is the most significant digit (100 MHz digit).

Table B-1. Phase Lock Loop Frequencies

Loop Name	Exact Frequency Range	Digits Controlled
High Frequency Loop	350 to 450 MHz*	8 and 9
N3 Loop	2.001 to 2.1 MHz	1 and 2
N2 Loop	19.8 to 29.79 MHz	3 through 5
N1 Loop	19.8 to 29.7 MHz	6 and 7
Sum Loop 2 (SL2)	20.0001 to 30 MHz	1 through 5
Sum Loop 1 (SL1)	20.000 001 to 30 MHz	1 thorugh 7

*To program 350 MHz, an 86601A, an 11707 or a jumper from mainframe J6 - Pin 43 to J6 - Pin 44 must be installed.

Figure B-2 shows how these tunable phase lock loops are combined in the mainframe to generate two tunable output signals that are mixed together in the RF section (and Frequency Extension Module) to produce the final output frequency.

The High Frequency Loop output is tunable in 10 MHz steps and the SL1 output is tunable in steps as small as 1 Hz.

The data needed to tune the phase lock loops to the proper frequencies is generated in the Digital Control Unit (DCU) in the mainframe. Frequency selection is done with thumbwheels or on a keyboard. Frequency stepping, sweeping and manual tuning is also controlled by the keyboard DCU. In the remote mode, frequency, modulation level and power output are controlled *through* the DCU. The frequency control data generated by the DCU is in a binary coded decimal (BCD) format in which a voltage greater than +2.4V is "on" and less than +0.8V is "off". (This is called high true or positive logic). The 2 MHz signal generated by the Reference Section is the main DCU clock.

The mainframe phase lock loop outputs are fed to either of two types of RF sections. (1) A low frequency RF section and (2) a high frequency RF section that requires the Frequency Extension Module to produce the final output frequency. We will explore the operation of these two types separately since they are distinctly different.

The low frequency RF Section, combines four mainframe signals to produce the final output frequency.

The 500 MHz fixed signal from the A4 Reference Section is mixed with a 20 MHz fixed signal from the Reference Section or a 20 MHz FM signal from the Modulation Section. The mixer output is filtered to yield the 480 MHz difference frequency. The 480 MHz is mixed with the SL1 loop output and filtered to produce 450 to 459.999 999 MHz which is mixed with the High Frequency Loop output to produce the final output frequency of 0 to 109.999 999 MHz. This signal is filtered, amplified, leveled and amplitude modulated (if selected) and fed to the output jack through the output attenuator. Figure B-3 blocks out the low frequency RF Section.

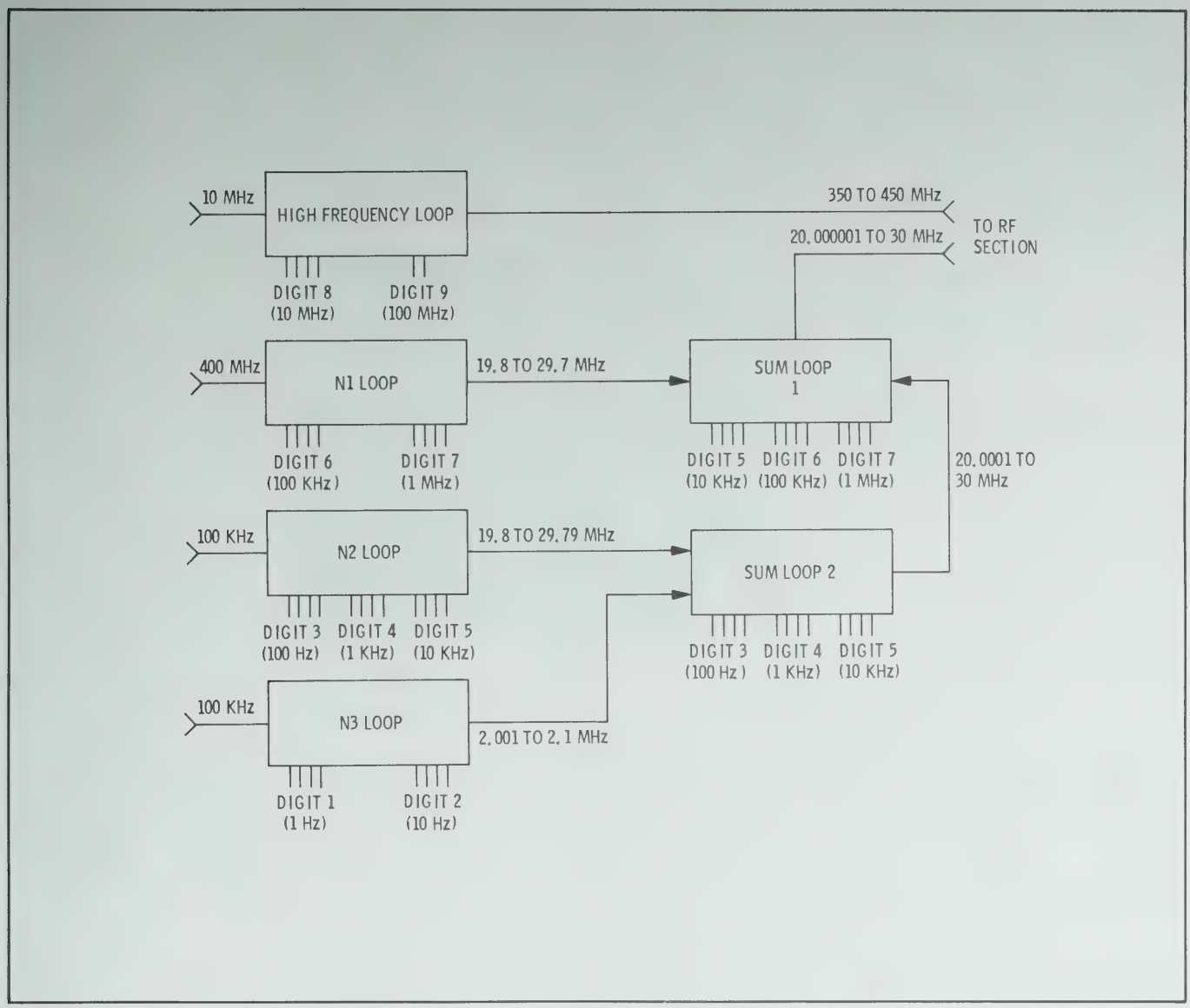


Figure B-2. 8660 Tunable Phase Lock Loops

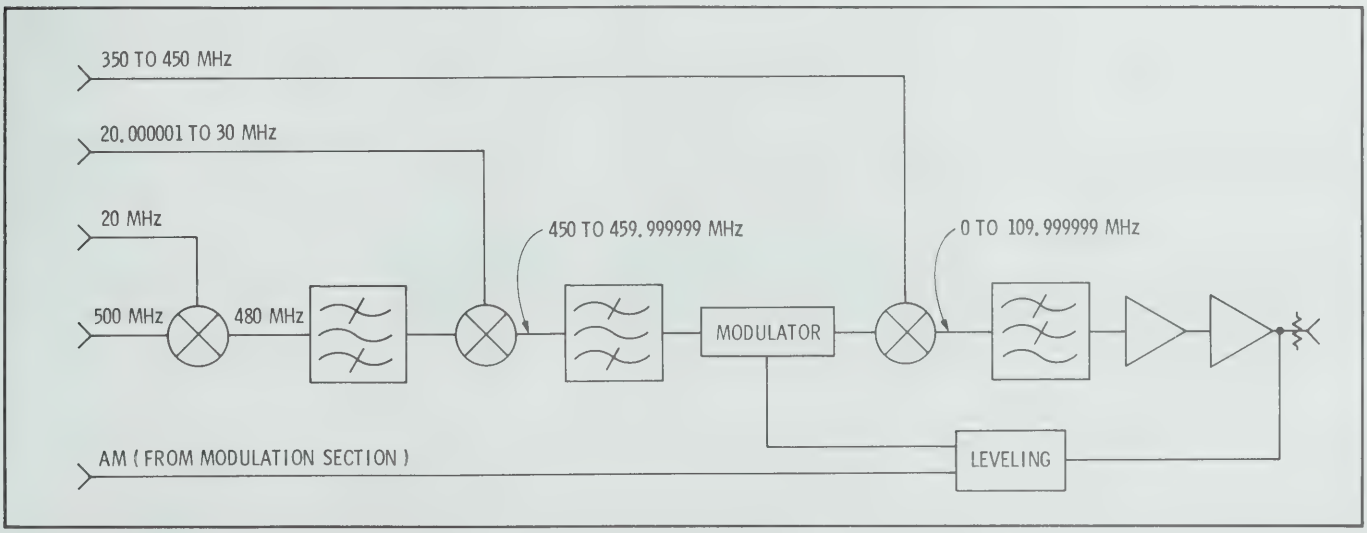


Figure B-3. Low Frequency RF Section

The High Frequency RF Section employs a Frequency Extension Module (FEM) to cover the added frequency range. There are two phase locked oscillators and one free running oscillator in the FEM. One of the phase lock oscillators operates over the range of 3.95 to 4.049 999 999 GHz ±5 MHz and the other produces 3.95 to 2.75 GHz ±5 MHz. These signals are combined in a mixer in the RF Section to produce 0 to 1299.999 999 MHz. The ±5 MHz tolerance is due to drift in the free running oscillator. This drift is cancelled in the mixer since both phase locked signals will be off frequency by precisely the same amount. Figure B-4 shows a block diagram of the FEM and high frequency RF section.

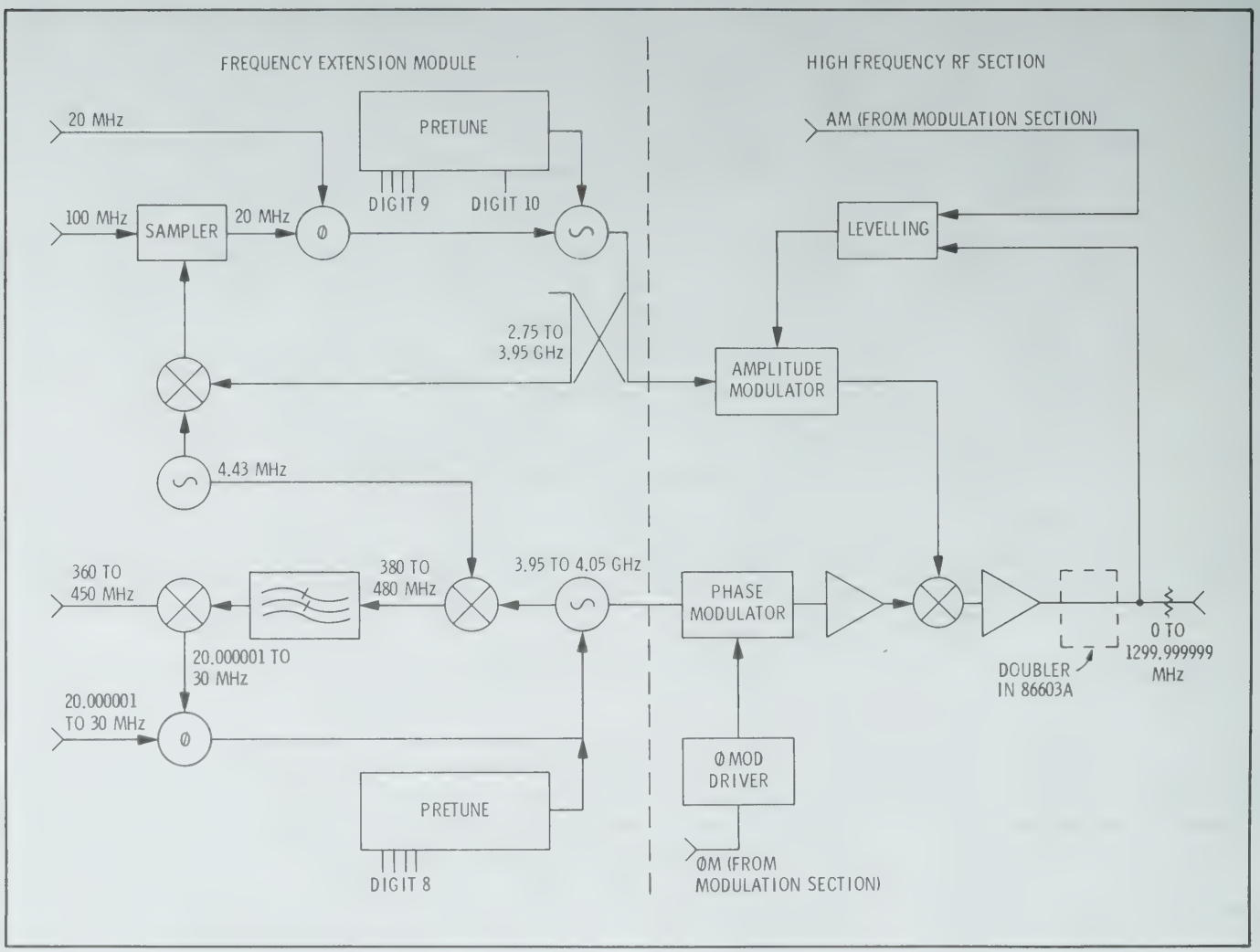


Figure B-4. Frequency Extension Module and High Frequency RF Section

In the 86603 High Frequency RF Section, a frequency doubler assembly extends instrument operation to 2599.999998 MHz. This doubler causes the minimum step size to be 2 Hz for frequencies above 1300 MHz.

The optional phase modulator in the 86603 operates as follows: the incoming 3.95—4.05 GHz signal from the FEM is fed through a four port circulator. Two of the ports are terminated by shunt varactor diodes. By changing the bias on the diodes the phase of the signals reflected from them can be varied and controlled. Each diode provides up to 55° of phase shift.

APPENDIX C
LOCATION OF TEST POINTS AND ASSEMBLIES

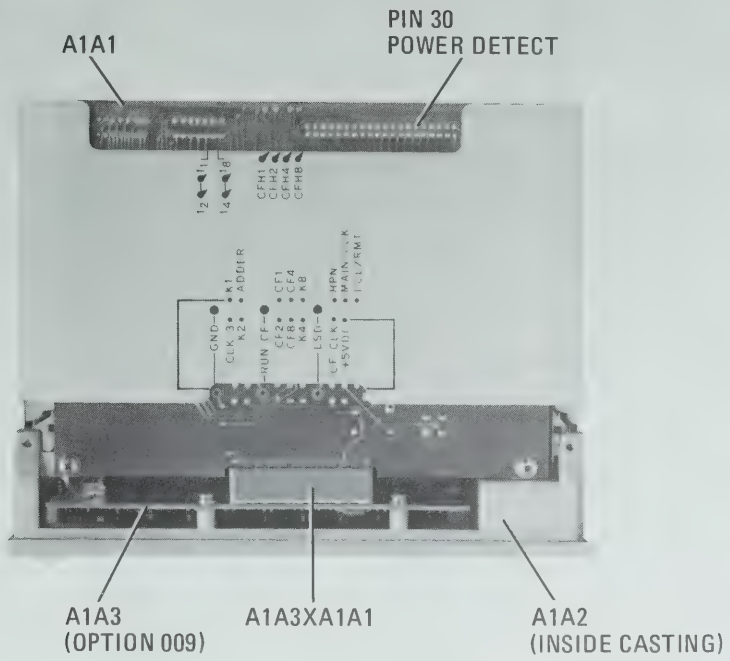


Figure C-1. 8660A Digital Control Unit, Top View

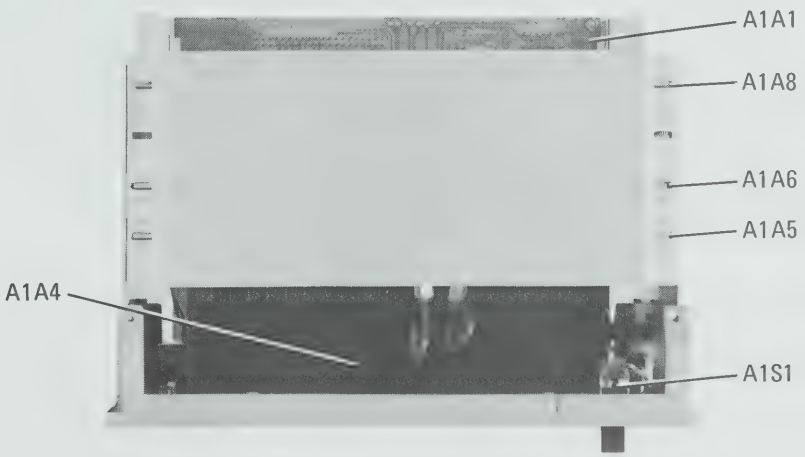


Figure C-2. 8660A Digital Control Unit, Bottom View

Test Points	Assemblies	Mother Board Inputs and Outputs
29 TP1 N3 Tuning Voltage 32 TP2 N3 10 kHz 31 TP3 N3 Phase Error 30 TP4 N3 Phase Error Grounding 26 TP5 SL2 Tuning Voltage 27 TP6 SL2 Oscillator Output 28 TP7 SL2 Pulse Phase Error 22 TP8 SL2 Phase Error 20 TP9 N2 Tuning Voltage 36 TP10 N2 Phase Error 37 TP11 N2 10 kHz 35 TP12 N2 Phase Error Grounding 16 TP13 SL1 Pulse Phase Error 15 TP14 SL1 Phase Error 39 TP15 N1 100 kHz 11 TP16 N1 Phase Error Grounding 13 TP17 N1 Phase Error 32 TP18 N1 Tuning Voltage 41 TP19 SL1 Mixer Output TP20 Not Connected 5 TP21 SL1 Tuning Voltage 8 TP22 SL1 Oscillator Output 10 N1 Oscillator Output XA17-1 pins 2 and D 19 N2 Oscillator Output XA13-1 pins 6 and 4 34 N3 Oscillator Output XA12-2 pin R 38 SL2 Oscillator Output XA15-2 pin 14	9 N1 Oscillator (A17) 12 N1 Phase Detector (A16) 18 N2 Oscillator (A13) 17 N2 Phase Detector (A14) 25 N3 Oscillator (A8) 24 N3 Phase Detector (A10) 23 SL2 Oscillator (A11) 21 SL2 Phase Detector (A12) 6 SL1 Oscillator (A19) 14 SL1 Phase Detector (A15) 7 SL1 Mixer (A18)	1 100 kHz Reference Input to N3 2 100 kHz Reference Input to N2 3 400 kHz Reference Input to N1 4 SL1 Output 33 BCD Frequency Data Digits 1 through 7

Figure C-3. 8660 Mainframe Mother Board Test Points (1 of 2)

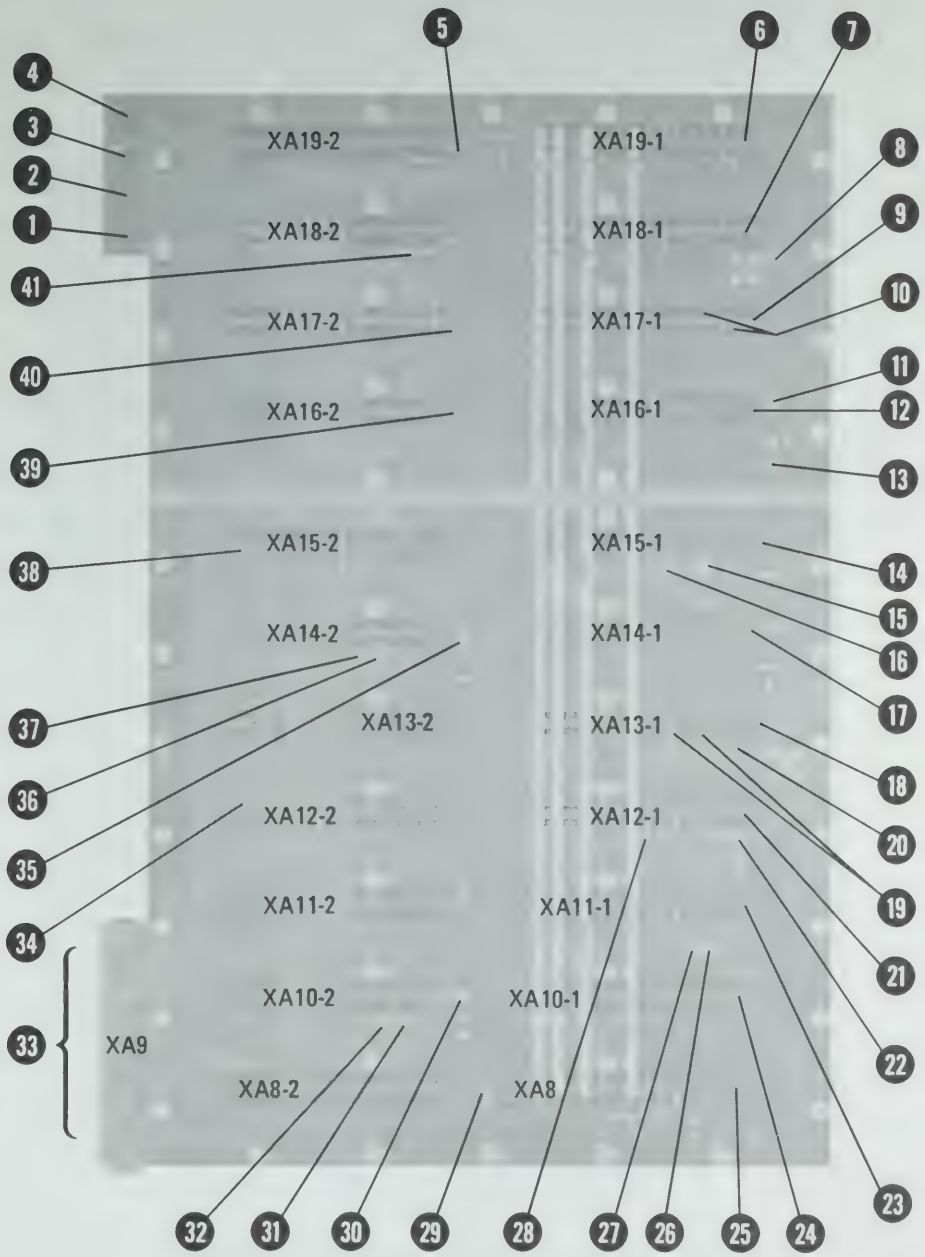


Figure C-3. 8660 Mainframe Mother Board Test Points (2 of 2)

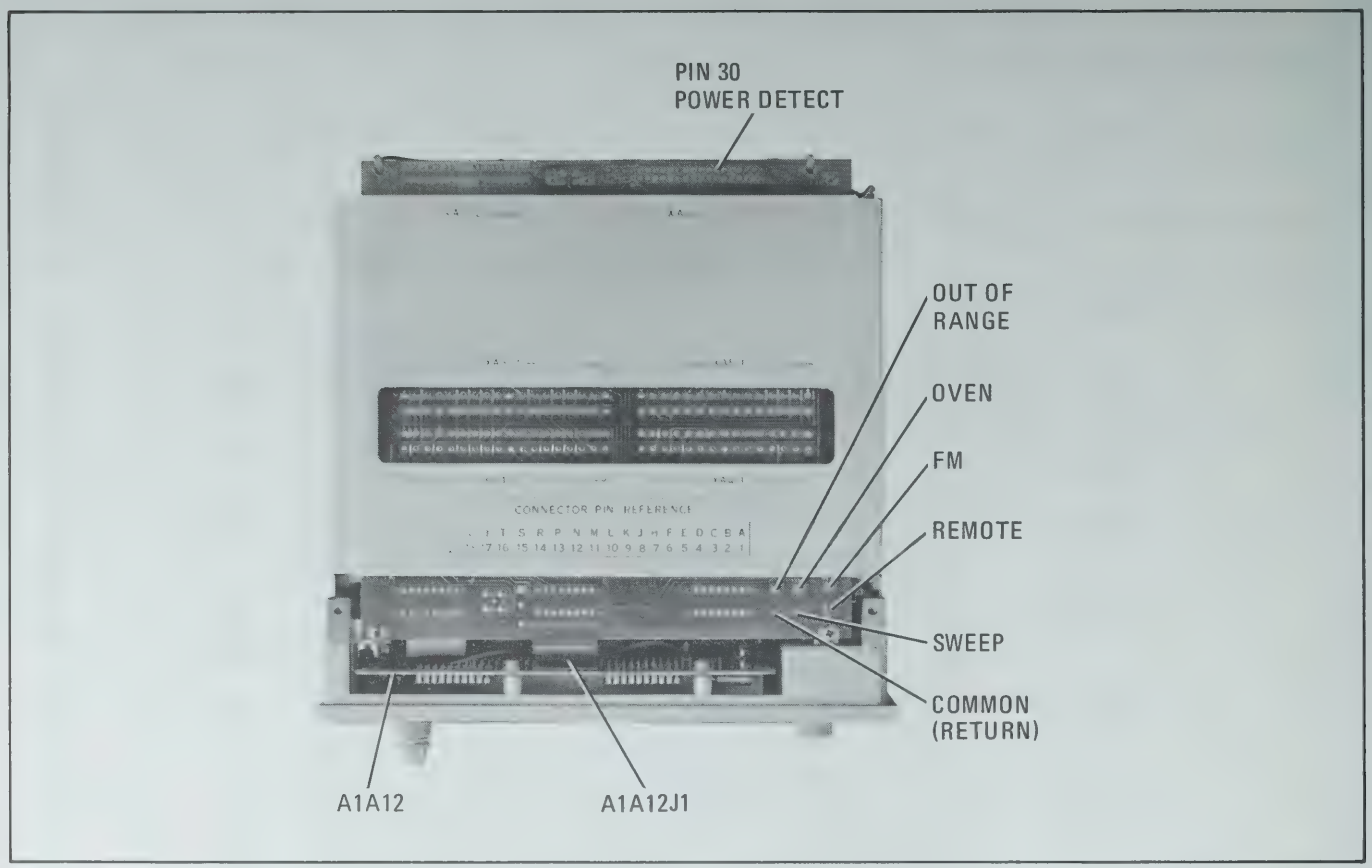


Figure C-4. 8660B/C Digital Control Unit, Top View

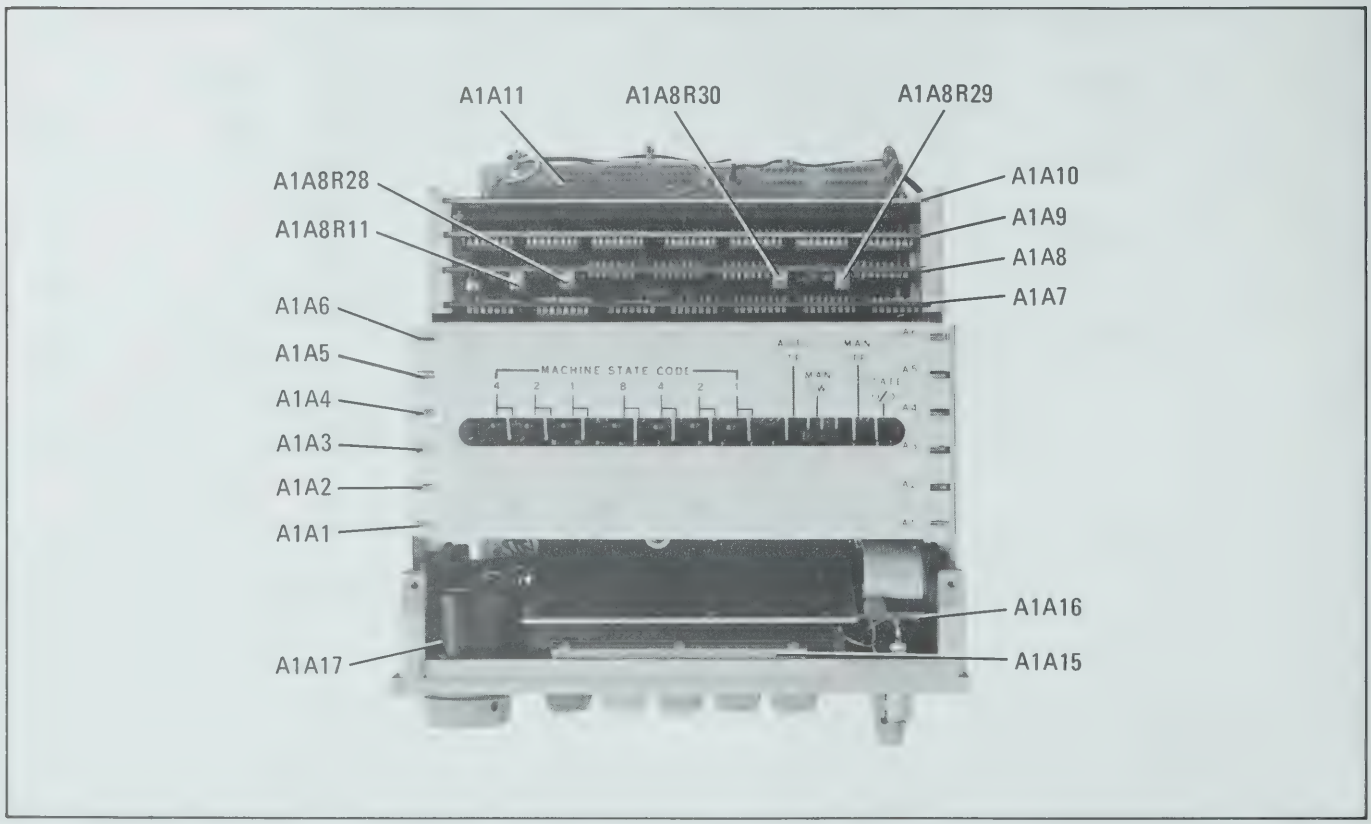


Figure C-5. 8660B/C Digital Control Unit, Bottom View

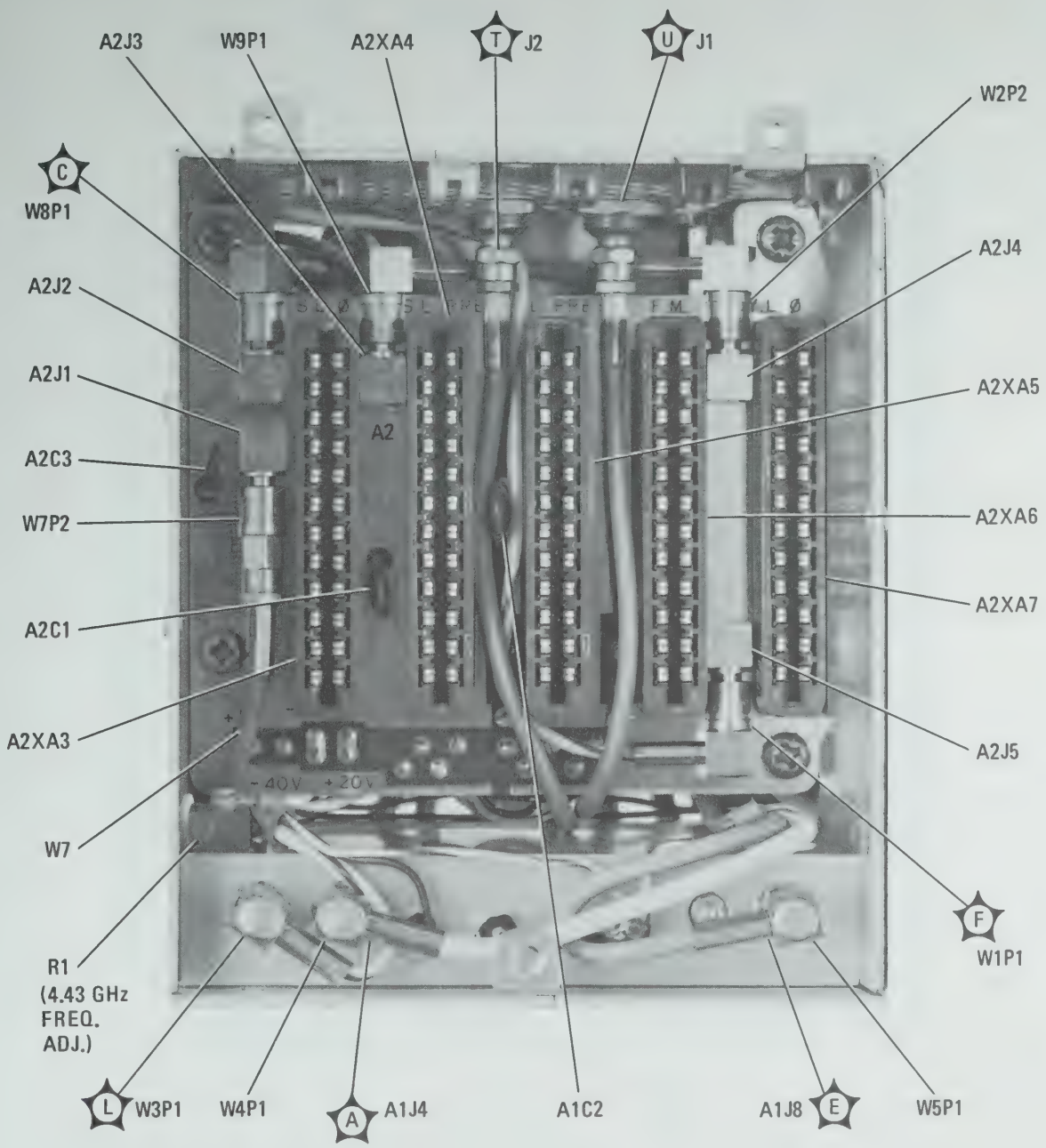


Figure C-6. 11661A Top View Test Points (1 of 2)

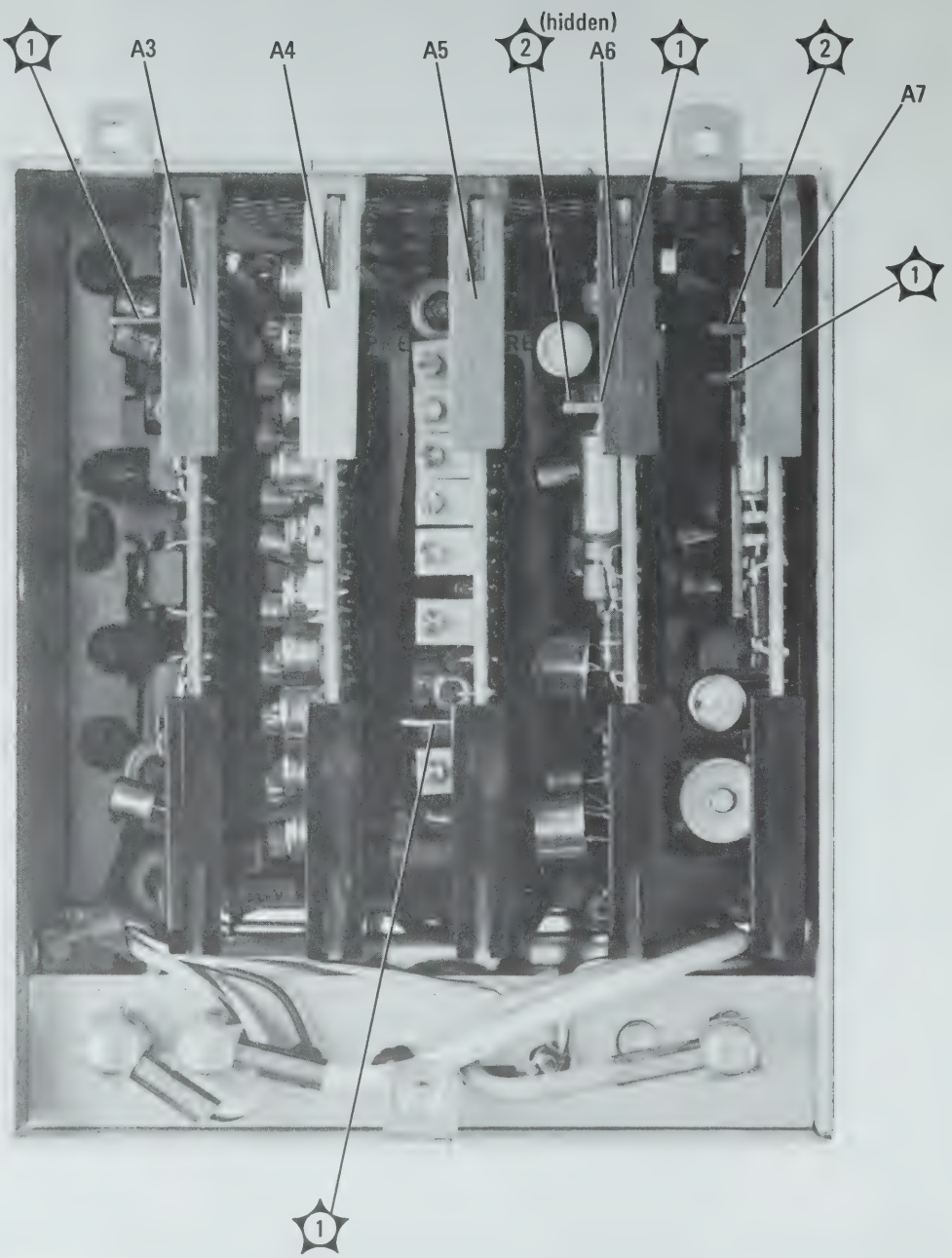


Figure C-6. 11661A Top View Test Points (2 of 2)

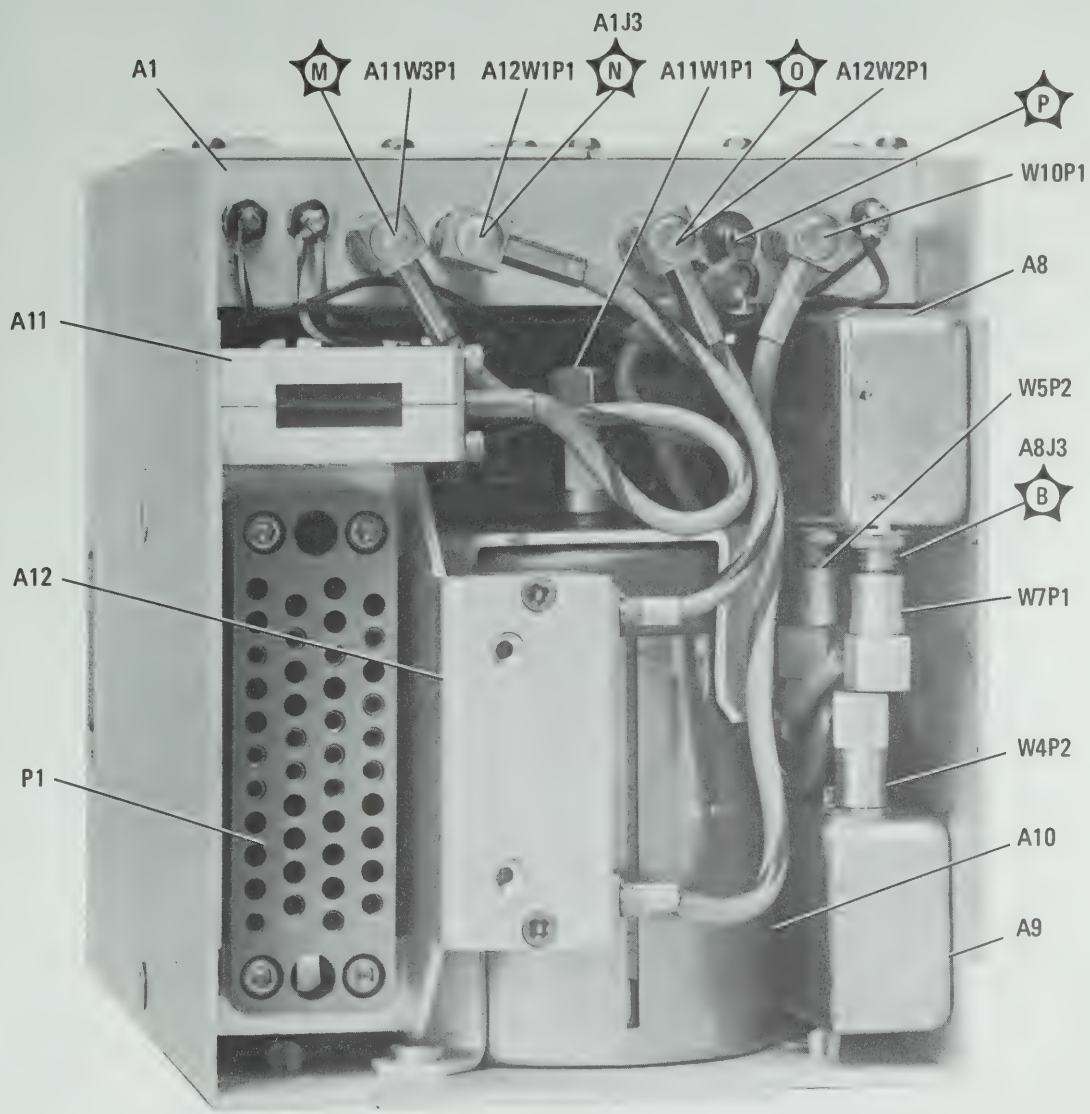


Figure C-7. 11661A Bottom View, Test Points and Assemblies

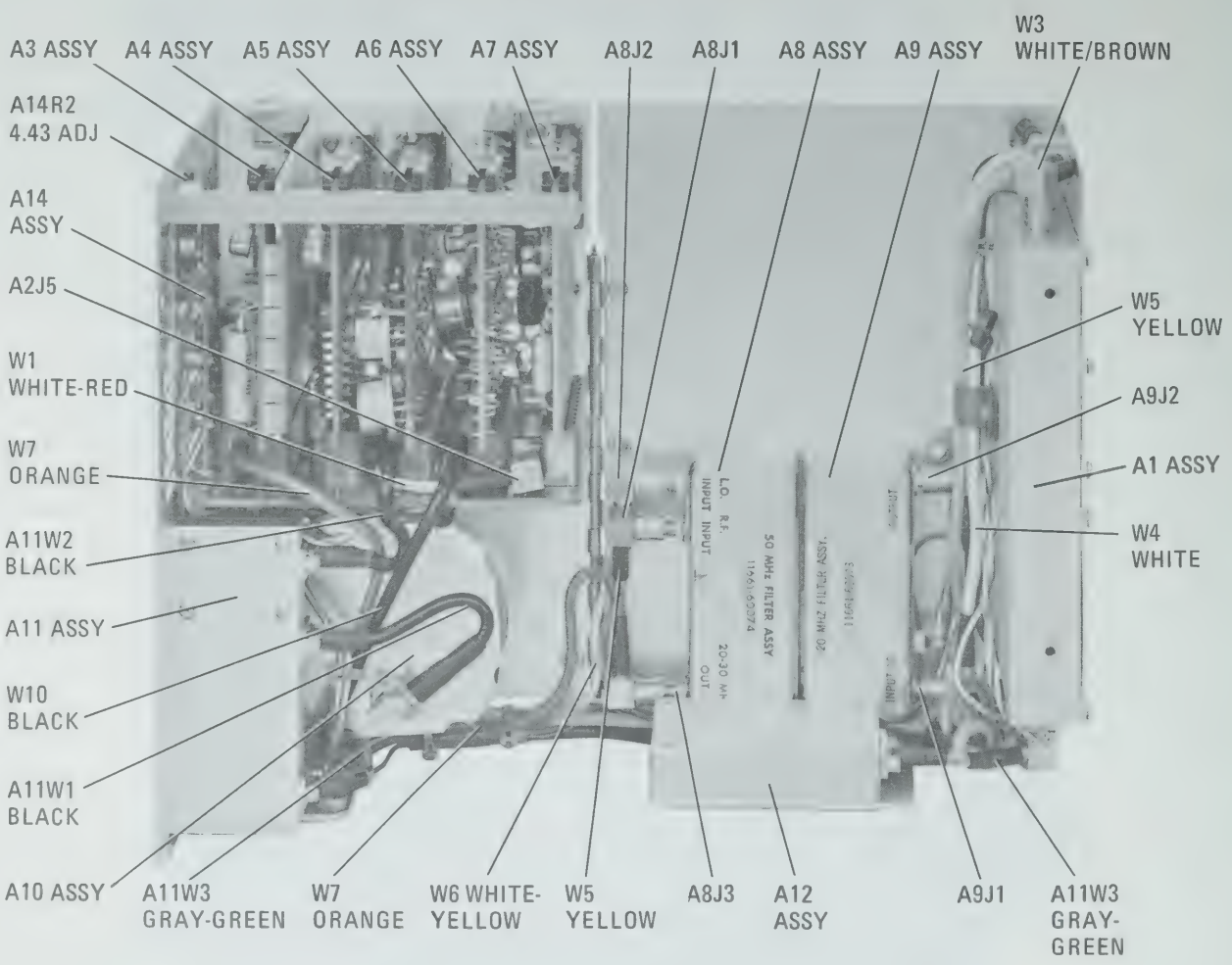


Figure C-8. 11661B Internal View

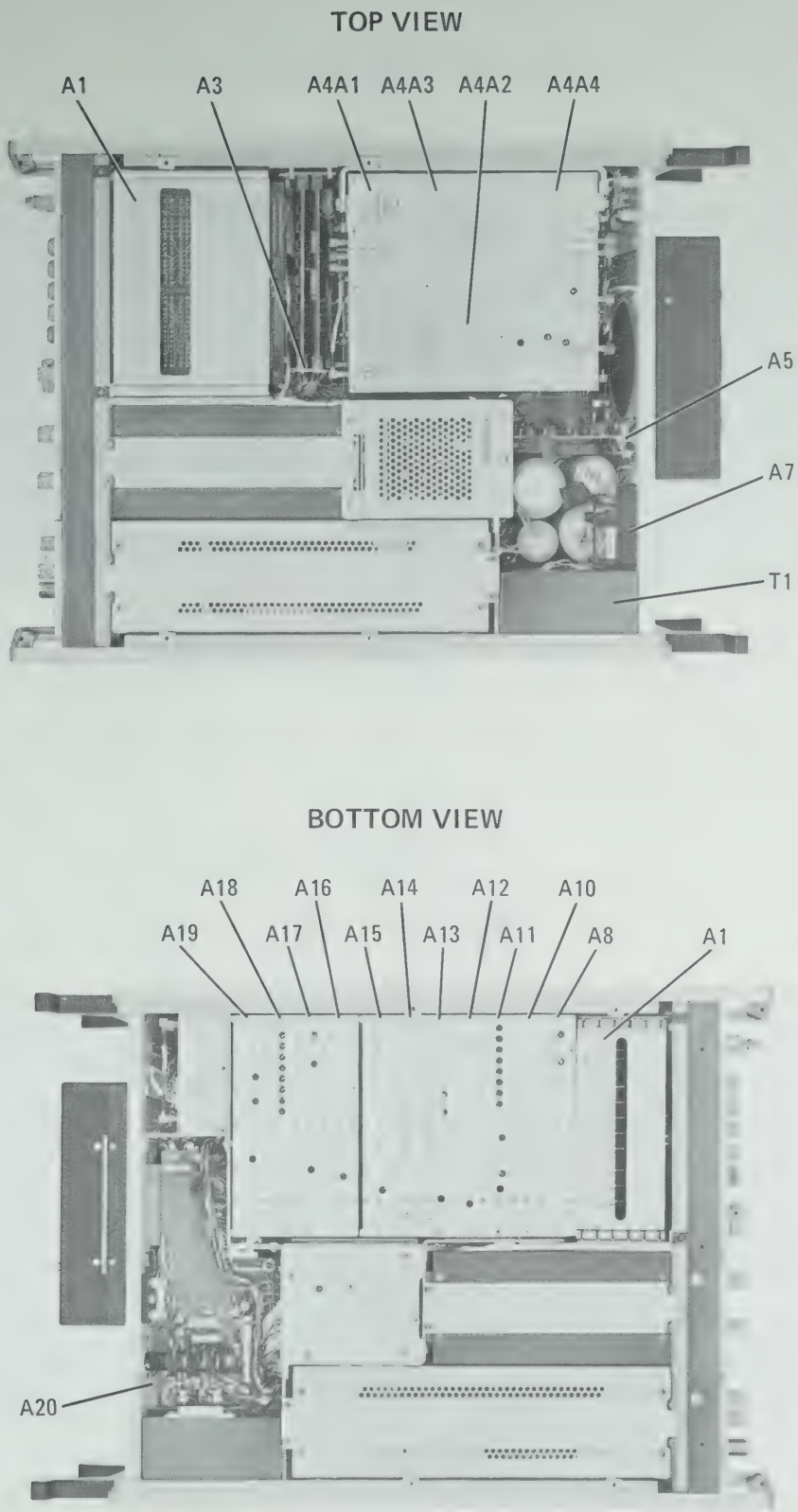
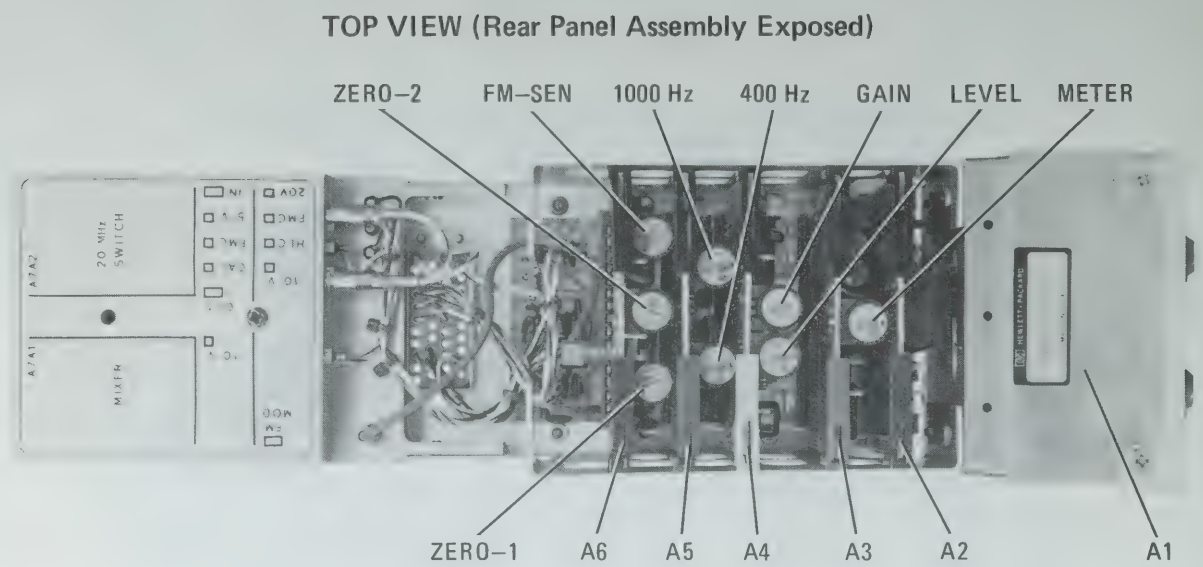


Figure C-9. 8660 Mainframe, Location of Major Assemblies



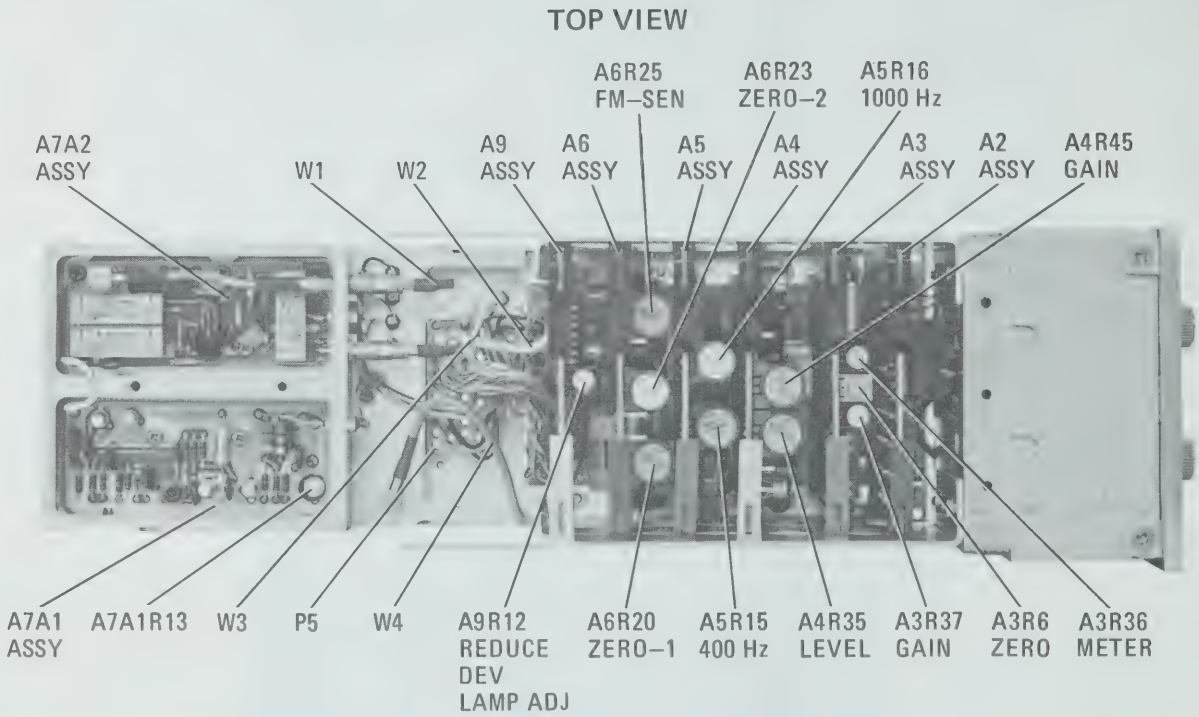


Figure C-10. 86632A and 86632B (86635A) Test Points and Assemblies

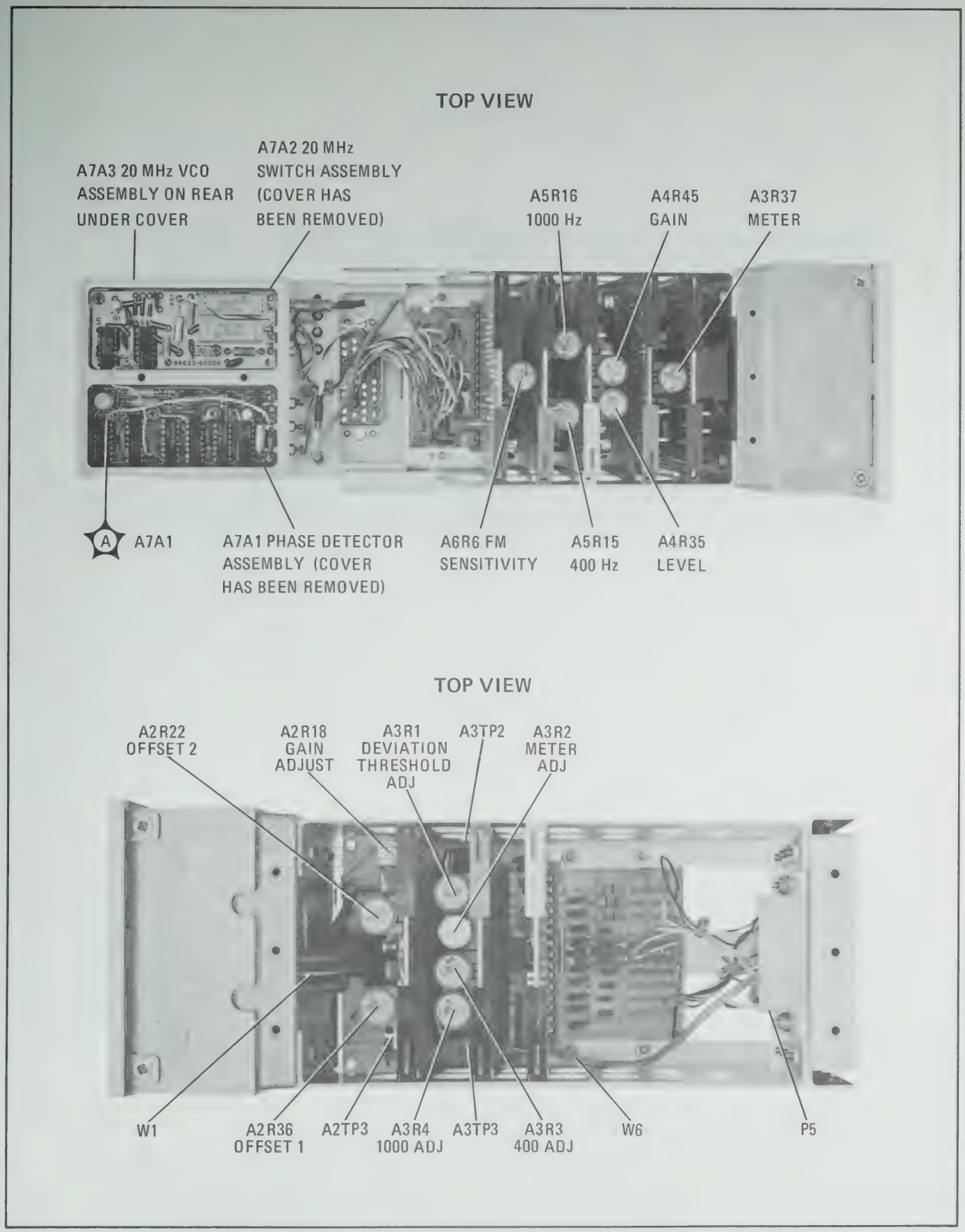


Figure C-11. Top Views of 86633A/B, 86634A.

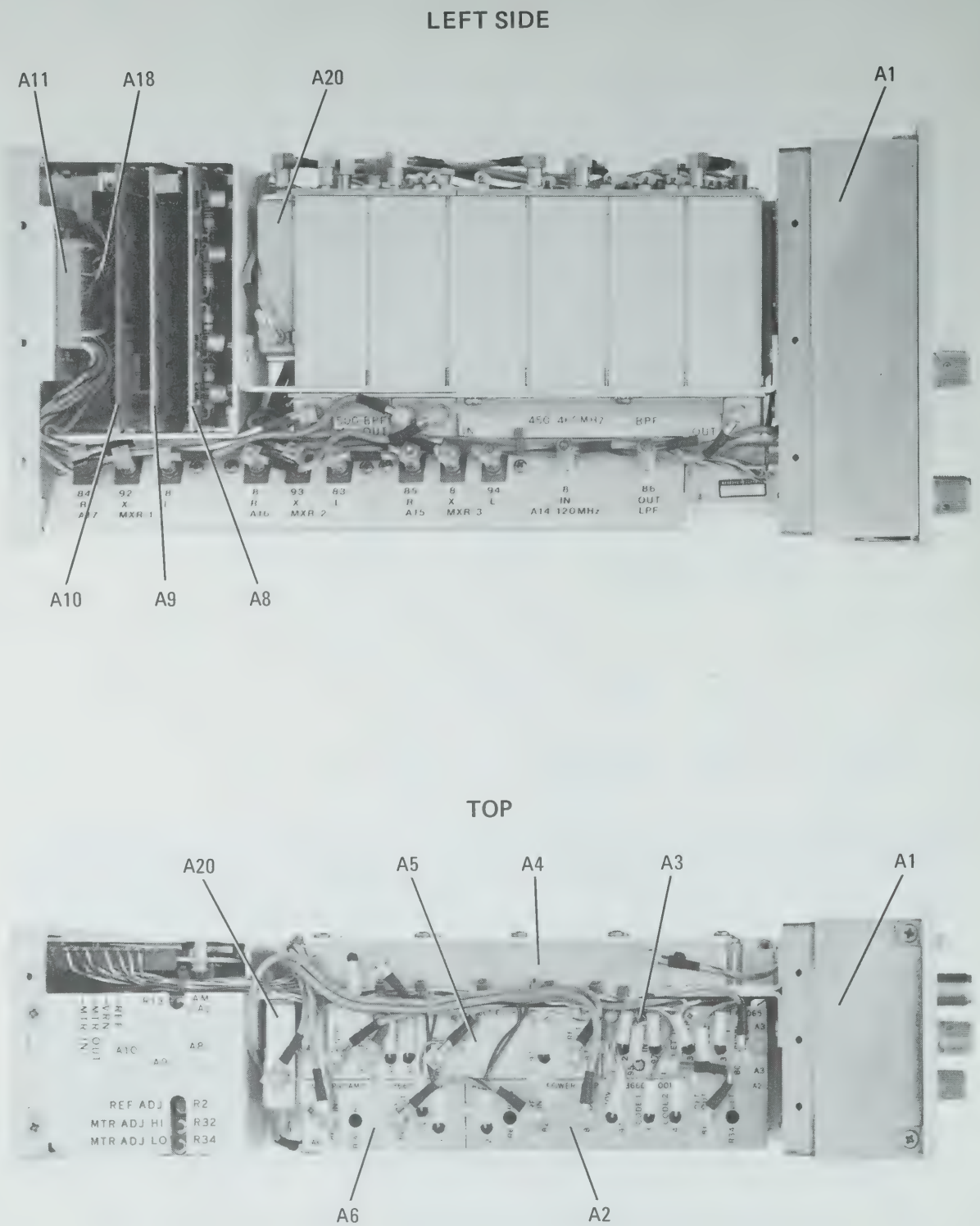


Figure C-12. 86601A Test Points and Assemblies (1 of 2)

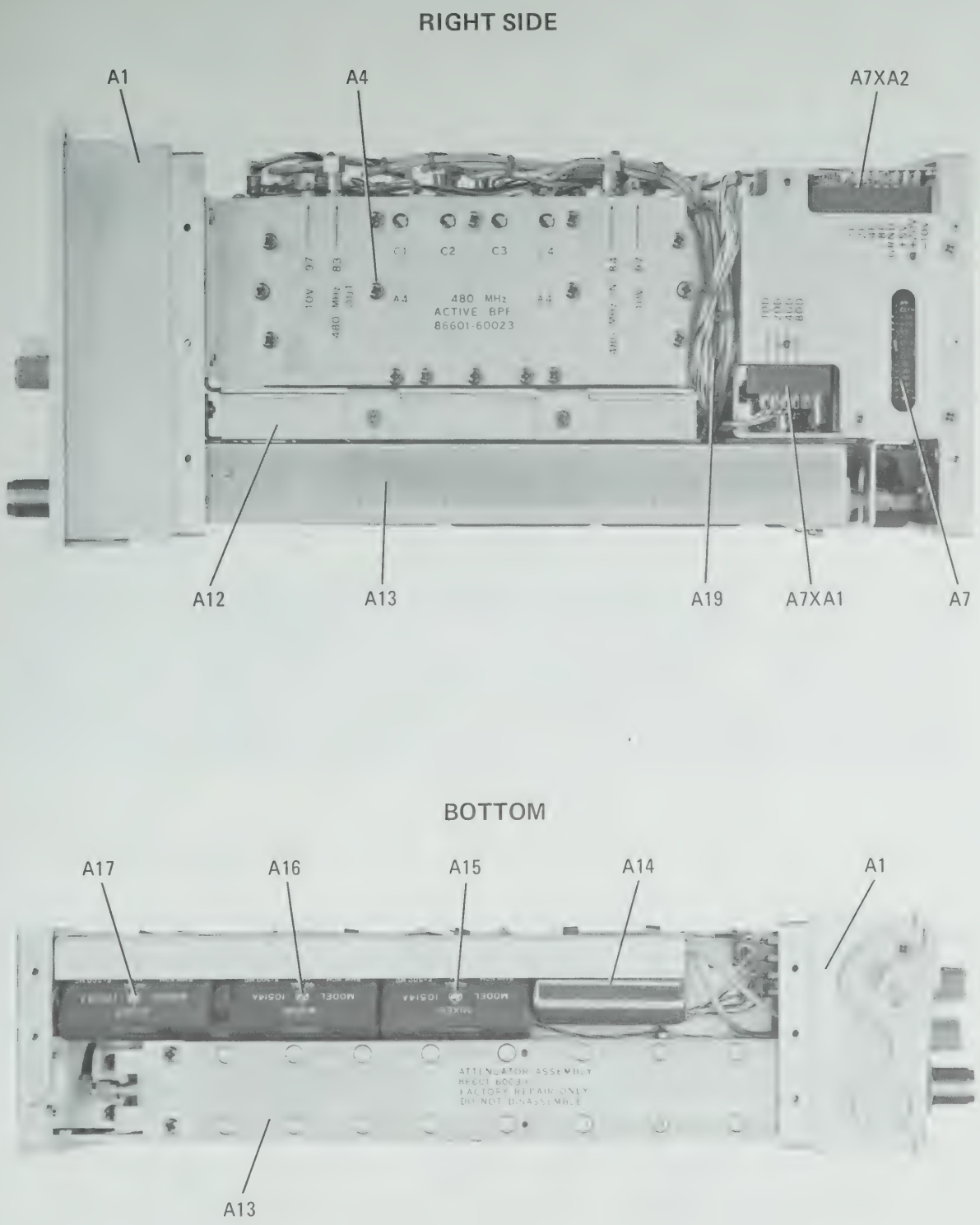


Figure C-12. 86601A Test Points and Assemblies (2 of 2)

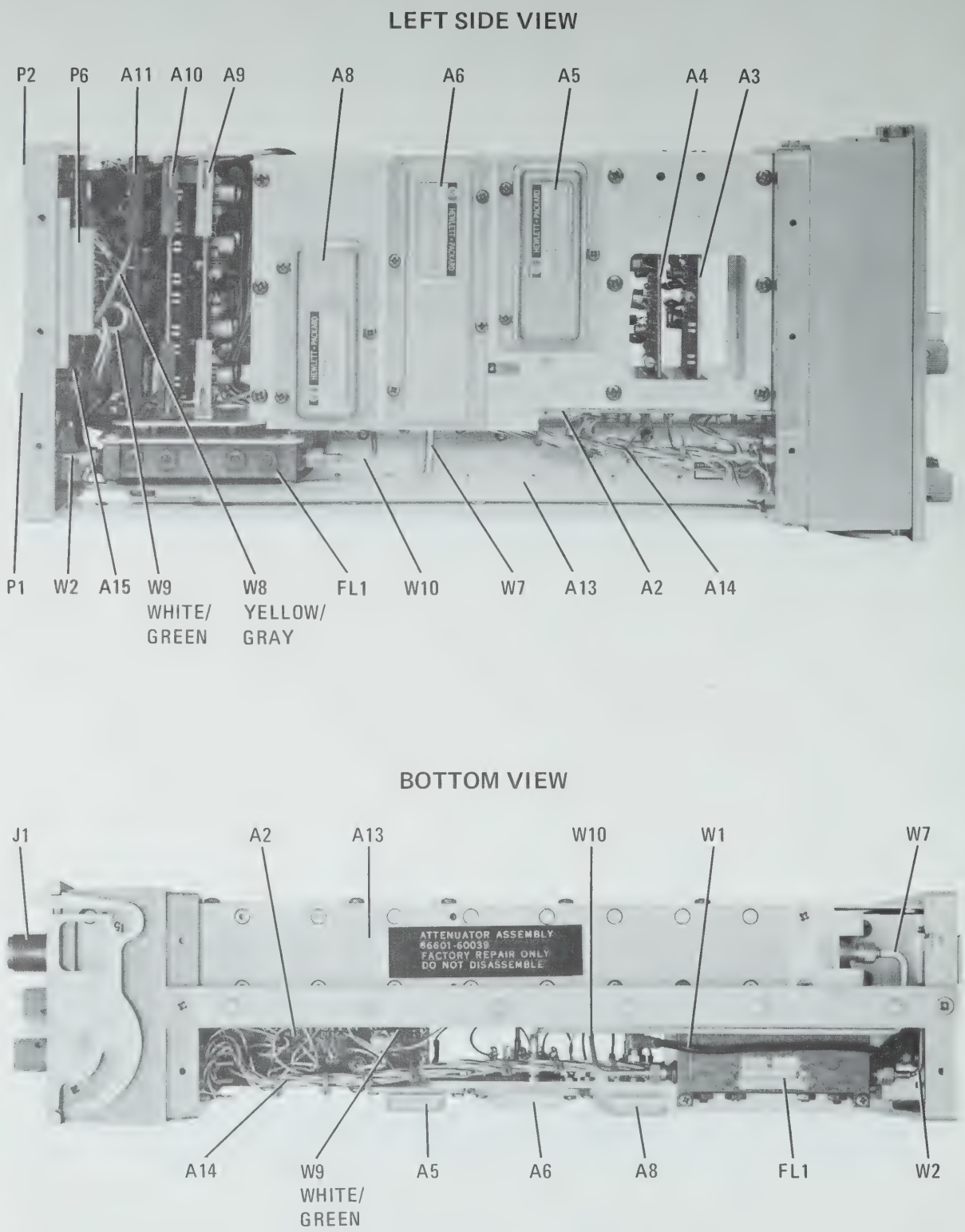


Figure C-13. 86602A Test Points and Assemblies (1 of 2)

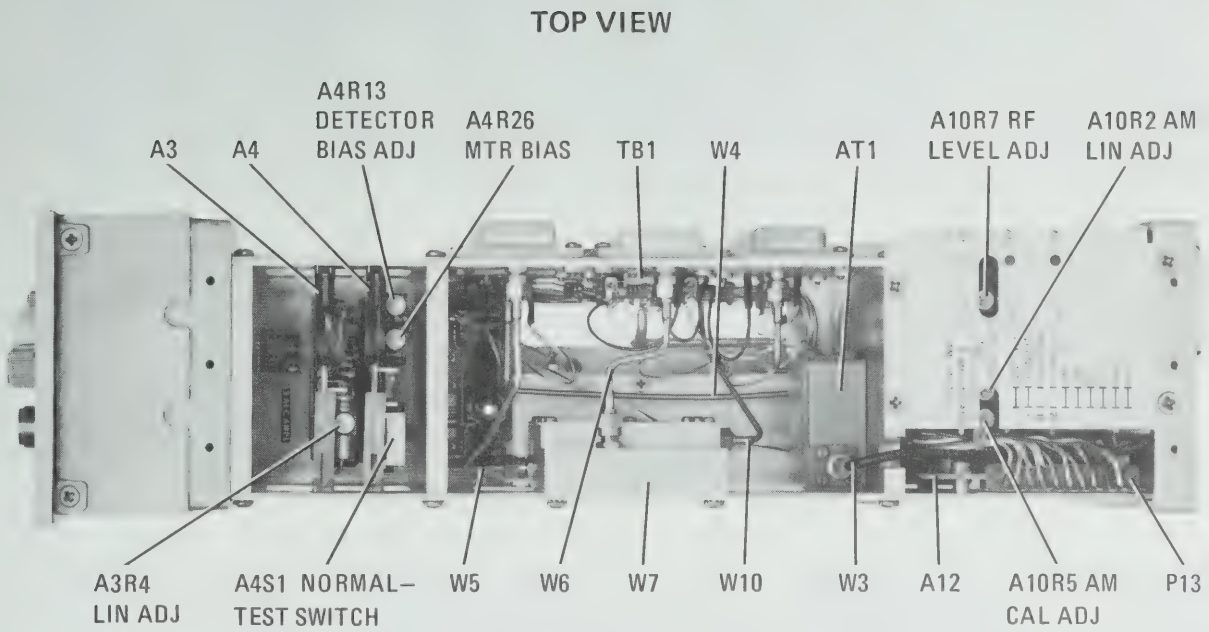
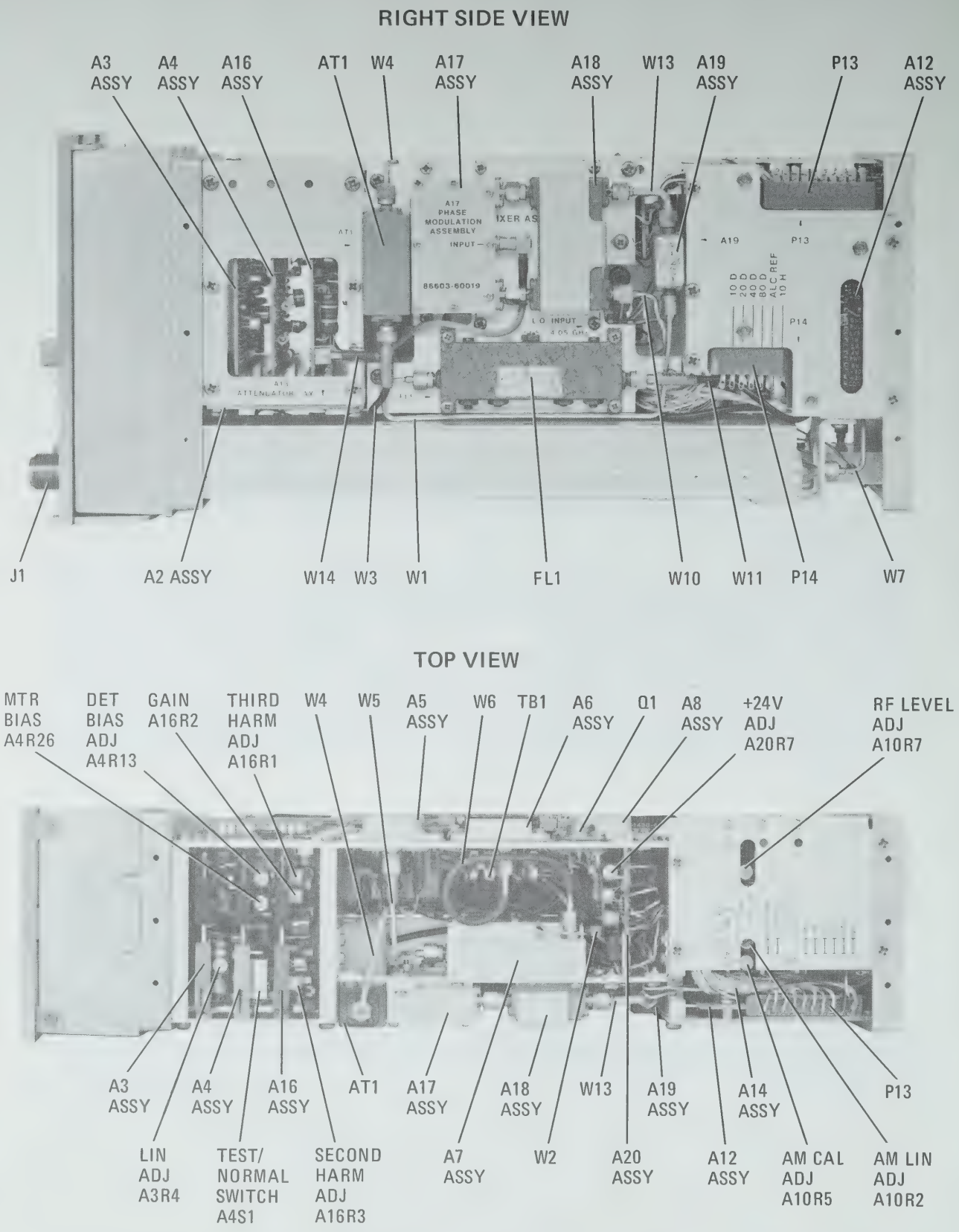


Figure C13. 86602A Test Points and Assemblies (2 of 2)



The 86602B is identical to the 86603A shown except there are no A20, A21, and A22 assemblies.

Figure C-14. 86603A (86602B) Test Points and Assemblies (1 of 2)

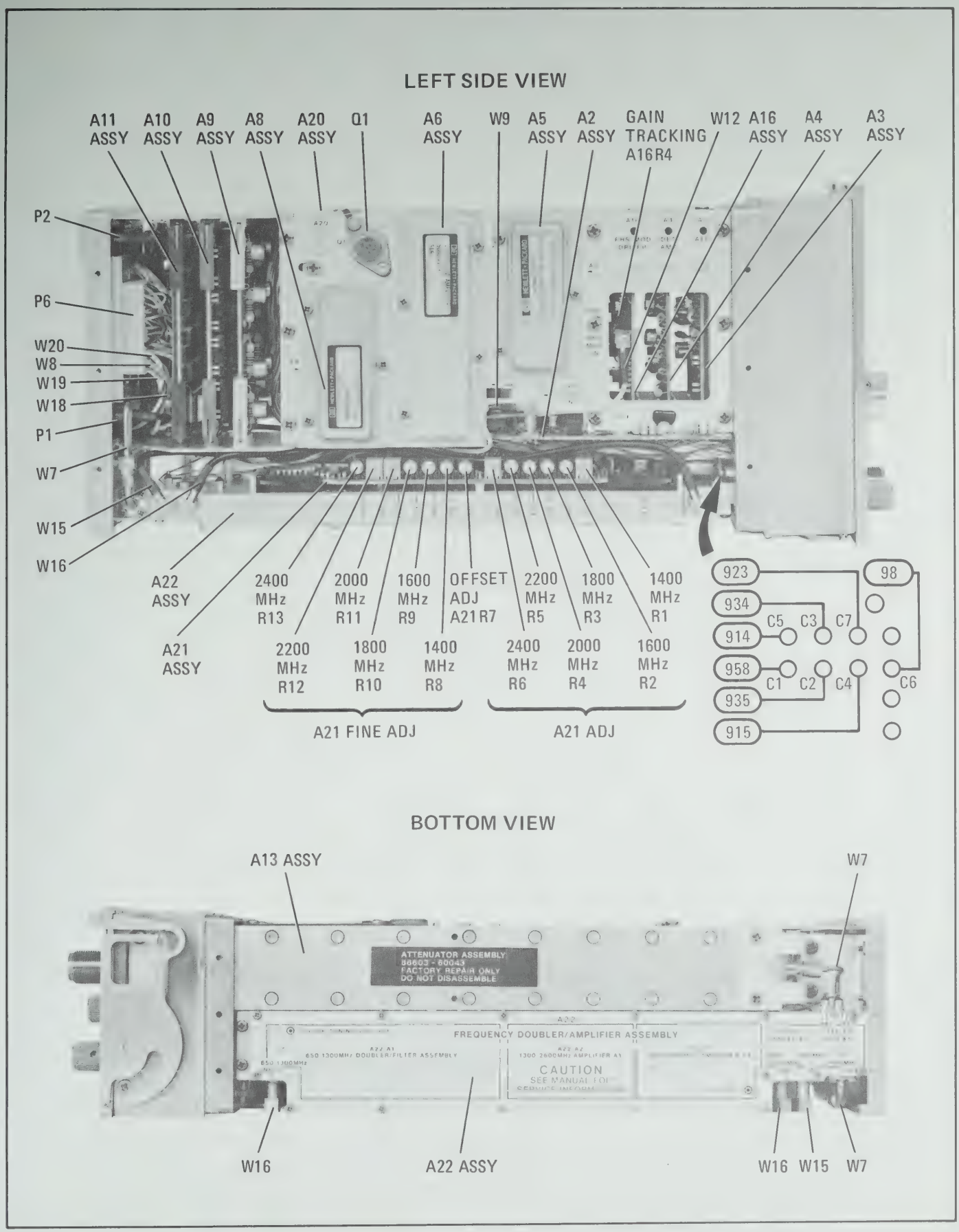


Figure C-14. 86603A (86602B) Test Points and Assemblies (2 of 2)

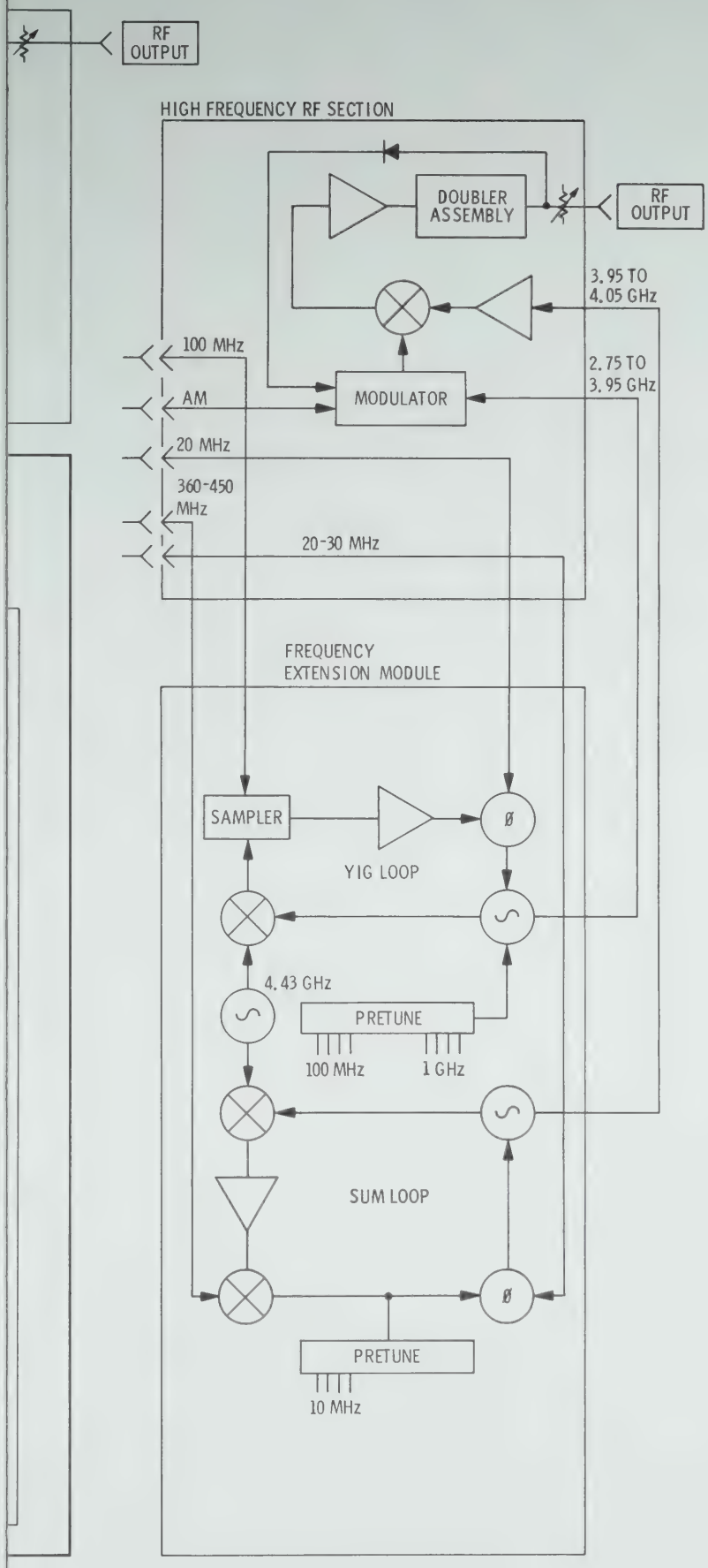


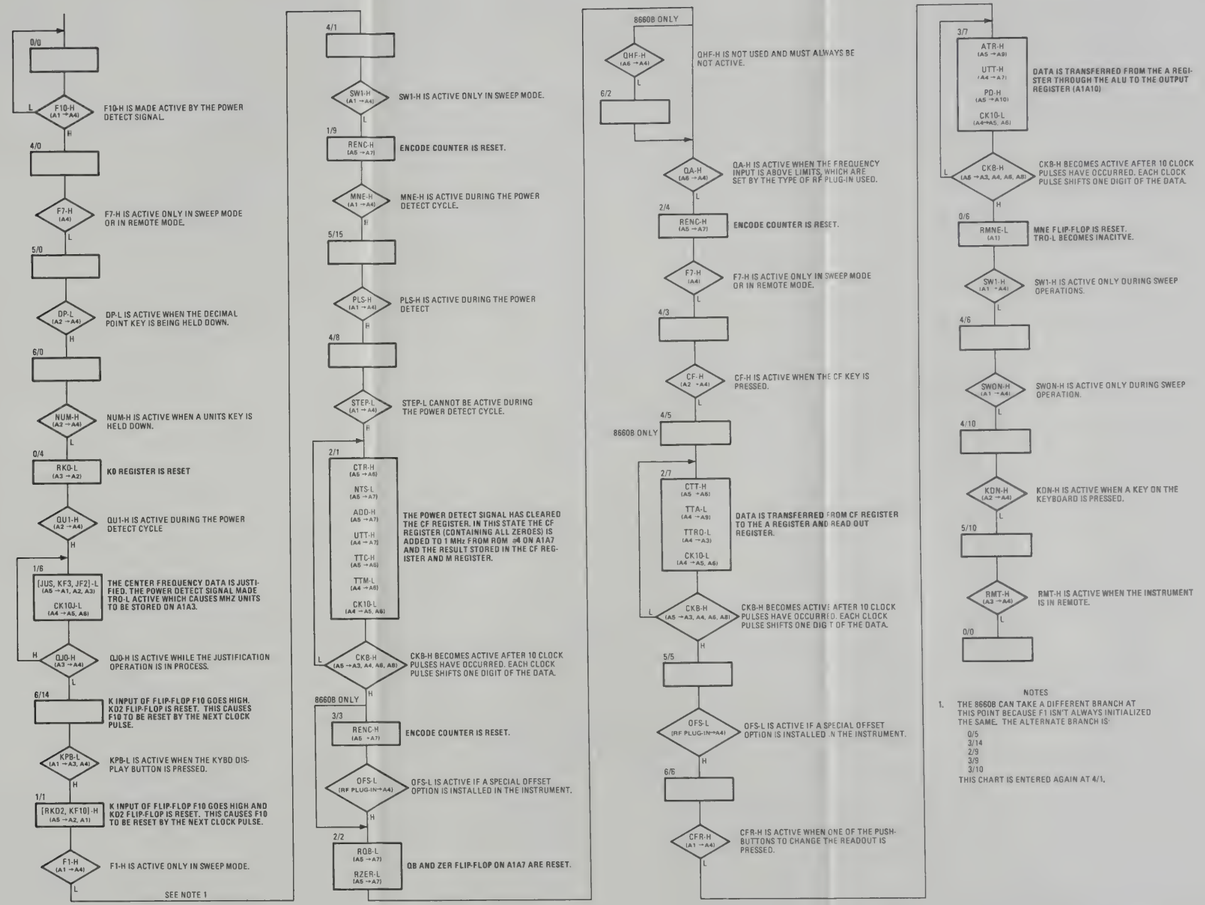
Figure D-1. System Block Diagram

POWER-ON INITIALIZATION DATA FLOW

When the power detect signal from the A3A1 assembly goes high, the ASM begins the power-on sequence. During state 1/6 MHz is stored as the units for the data. When state 2/1 is reached, the CF Register (which was cleared by the power detect signal) is added to 1 MHz from ROM #4 on the ALU board and the result stored in the CF and M Registers. During state 2/7 the data in the CF Register is transferred to the Read Out and A Registers. Then when state 3/7 is reached, data is transferred from the A Register to the Output Register.

HOW TO USE

1. Turn the LINE switch to STBY.
2. Connect a test lead from ground to the DCU MAN TP.
3. Turn the LINE switch to ON.
4. Single step the ASM using the MAN SW and check using the troubleshooting flow chart.



NOTES

1. THE 8660B CAN TAKE A DIFFERENT BRANCH AT THIS POINT BECAUSE F1 ISN'T ALWAYS INITIALIZED THE SAME. THE ALTERNATE BRANCH IS:
   0/5
   3/14
   2/9
   3/9
   3/10
   THIS CHART IS ENTERED AGAIN AT 4/1.

Figure 12-12. ASM Troubleshooting Flow Chart for Power-On Initialization

APPENDIX E
11661 TEST BOARD

Troubleshooting the 11661 phase lock loop circuit boards A3, A6 and A7 can be simplified by constructing a simple test board. This board uses a standard extender board, Hewlett-Packard part number 5060-0258, and four small SPDT toggle switches, HP part number 3101-0163 or equivalent.

INSTRUCTIONS FOR CONSTRUCTION

1. Open connections to blue ribbon (edge) connector pins A, B, 10 and 11 from extender board lines.
2. Mount switches on lettered side of board.
3. Wire as shown in Figure E-1.
4. Put a label as shown below on the lettered side of the circuit board to show switch positions.

Switch	11	10	B	A
Normal	/	/	/	/
Test A3 (Green)	/	/	\	/
Test A7 (Brown)	/	/	/	\
Test A6 (Red)	\	\	/	/

5. This board is used for component level troubleshooting. Remove all other boards when using this test board.

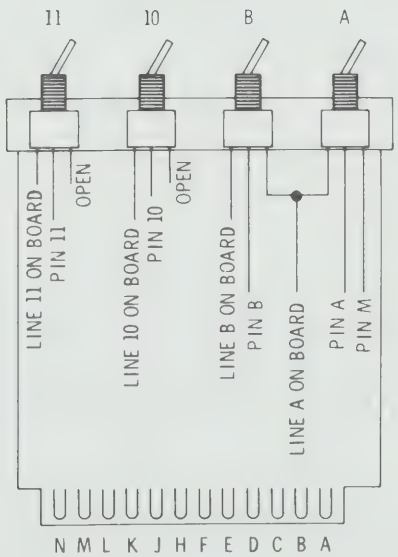


Figure E-1. 11661 Test Board

APPLICATION

A3

The switches tie the two 20-30 MHz inputs together and to the SL1 mainframe signal. In this state, A3TP1 should be approximately 10 Vdc.

A6

The switches open the output lines to the YIG oscillator's FM coil.

A7

The switches connect the YIG loop phase detector inputs both to the 20 MHz mainframe reference. In this state A7TP2 should be 0V ± 0.1 Vdc.

APPENDIX F
KEYBOARD DISASSEMBLY AND REPAIRS

The keyboard (A1A15) of the 8660B and 8660C mainframes can easily be disassembled and repaired, rather than being replaced as an assembly. Figure F-1 shows an exploded view of the keyboard as an aid to identifying any part that may be needed.

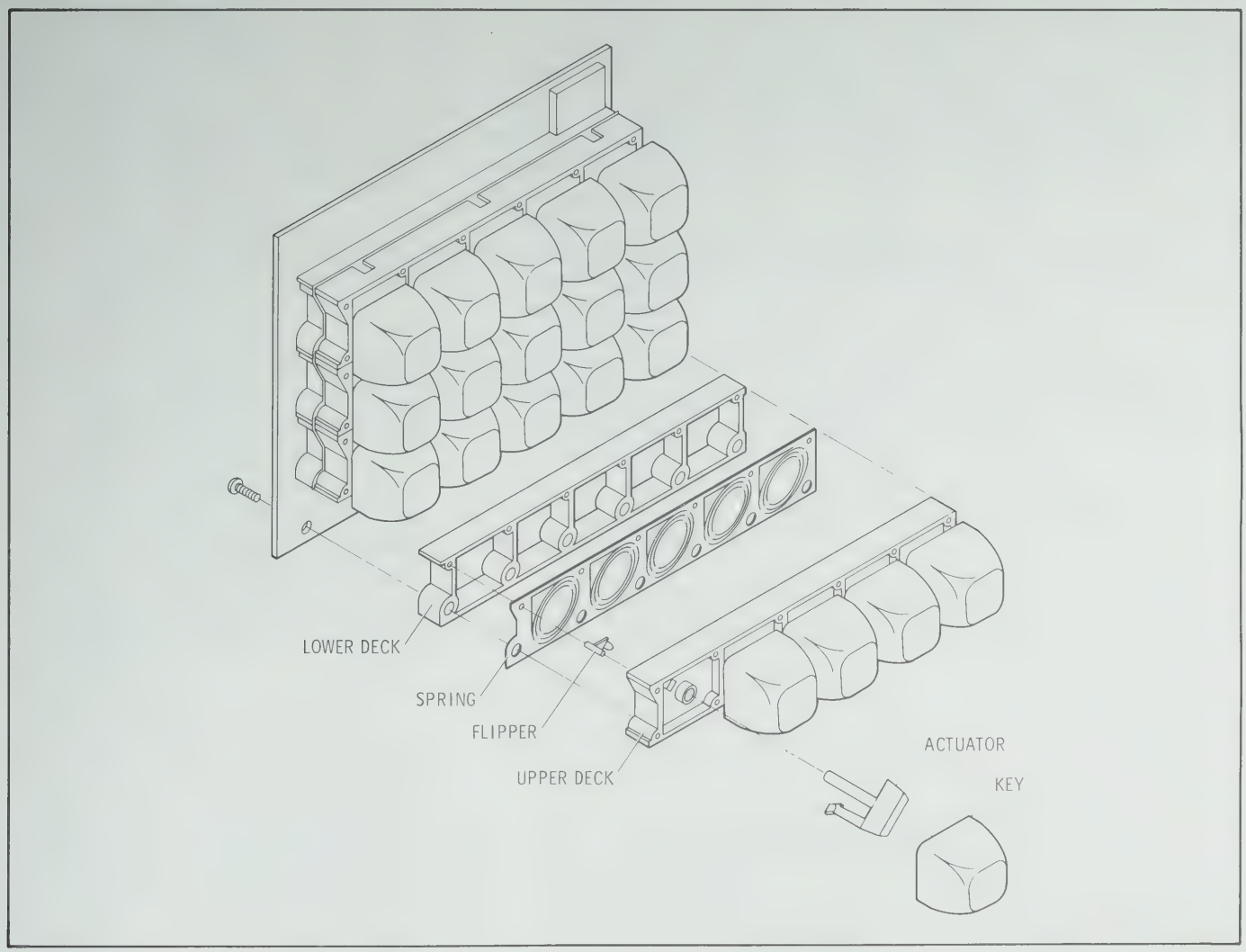


Figure F-1. 8660B and 8660C Keyboard IPB

It is not unusual for keys to stick on this keyboard. Usually no new parts are required to repair this problem. Follow this procedure:

1. Pull off the offending key.
2. Carefully pry the actuator stems and pull out the actuator.
3. File or sand the main stem to remove any rough spots and wipe the stem clean.
4. Reinstall the actuator and press the key into place. (Make sure it's right side up!)

Replacement part numbers for the keyboard are shown in Table F-1.

Table F-1. Keyboard Replacement Parts

Qty	Description	HP Part Number
20	Actuators	5050-6942 (new)
20	Flippers	5040-6941 (new)
4	Upper Decks	5040-0364
4	Lower Decks	5040-0365
4	Springs	5001-0109
1	Key, Number 1	5040-6902
1	Key, Number 2	5040-6903
1	Key, Number 3	5040-6904
1	Key, Number 4	5040-6905
1	Key, Number 5	5040-6906
1	Key, Number 6	5040-6907
1	Key, Number 7	5040-6908
1	Key, Number 8	5040-6909
1	Key, Number 9	5040-6910
1	Key, Number 0	5040-6911
1	Key, Decimal Point	5040-6901
1	Key, Clear KYBD	5040-6912
1	Key, STEP↑	5040-6913
1	Key, STEP↓	5040-6014
1	Key, SWP WIDTH	5040-6915
1	Key, CF	5040-6916
1	Key, Hz	5040-6917
1	Key, MHz	5040-6918
1	Key, kHz	5040-6919
1	Key, GHz	5040-6920

APPENDIX G
MODULATION ACCURACY AND DISTORTION

A procedure for isolating the source of modulation accuracy and distortion problems is given in this appendix.

For AM problems begin at step G1.

For FM problems begin at step G-8.

For ϕM problems begin at step G-13.

G-1. Attach spectrum analyzer to RF output. Set AM 30% 1000 Hz. The first sidebands should be 16.4 dB below the carrier. AM accuracy must be correct before checking distortion. If OK, skip to step G-4 to check distortion. If not OK, remove the RF section and substitute an 11707 Test Plug-in (if an 117707 is not available the voltage to be tested is at mainframe J6 coax pin 55. See Figure G-1 for setup).

G-2. Set the modulation section to indicate 100% AM. Set the 11707 DC/MOD switch to AM. Attach a digital voltmeter to the 11707 DC/MOD test jack, or to J6 pin 55. Should measure 1 ± .01 Vrms (2.8 ± .028 Vpp).

G-3. If the voltage is correct, perform the AM calibration adjustments in Section V of the RF Section Operating and Service Manual. If the adjustments don't solve the problem, troubleshoot the RF Section AM input circuitry (A9 in 86601, A10 in 86602 and 86603) or the RF Section ALC circuitry (A3 in all RF sections).

G-4. If all OK through this step, AM accuracy is correct. Do the Amplitude Modulation Distortion Performance Test in the RF Section of the Operating and Service Manual.

G-5. If the AM Distortion is out of specifications, remove the RF Section and substitute an 11707 Test Plug-in. (If an 11707 is not available connect to mainframe J6 pin 55 as shown in Figure G-1.)

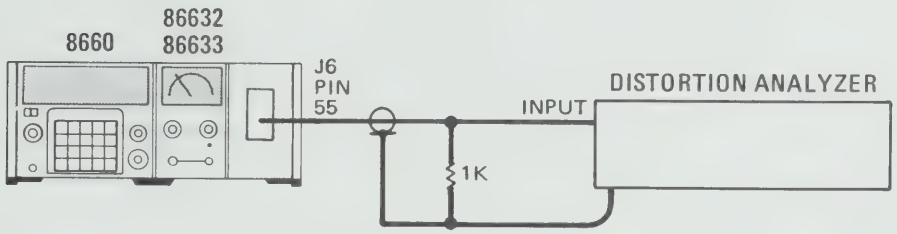


Figure G-1. AM Measurements

G-6. Set Modulation Section to AM INTERNAL 1000 Hz and set 100% meter reading.

G-7. Use distortion analyzer to measure total harmonic distortion. Distortion should be less than 1%. If distortion is not within this limit, troubleshoot the AM portions of the modulation section after checking the ripple of the mainframe power supplies. If modulation section distortion is OK, troubleshoot the AM portions of the RF Section to isolate the source of the distortion.

G-8. *FM Problems.* Set Modulation Section MODE to FM and MODULATION LEVEL to minimum. Remove RF Section and using coax pin HP Part No. 11672-60008, and a power meter measure the power out of Mainframe J6 pin 62. Should be approximately −4 dBm minimum. This signal should be about 340 mVpp on an oscilloscope at 20 MHz.

G-9. If the 20 MHz signal is OK, disconnect the adapter from J6 and install an 11707 Test Plug-in. If the 20 MHz signal is not OK, skip to G-12.

G-10. Attach spectrum analyzer to 20/FM jack of 11707. Set 86632 (86633 settings in parentheses) or 86635 Modulation Section to FM x 10 (FM x 1) EXTERNAL AC attach 651B, 600 ohm output to modulation input. Set 651B to exactly 415.834 kHz (41.583 kHz) as monitored on a frequency counter. Set 651B output level to about 1 Vrms. Set modulation level to reach the first carrier null as viewed on spectrum analyzer. The 86632 or 86635 (86633) meter should indicate 1 MHz (100 kHz) peak deviation ±50 kHz (5 kHz).

G-11. If the FM Accuracy is correct, check the FM Distortion from the modulating section by using the test setup shown in Figure G-2.

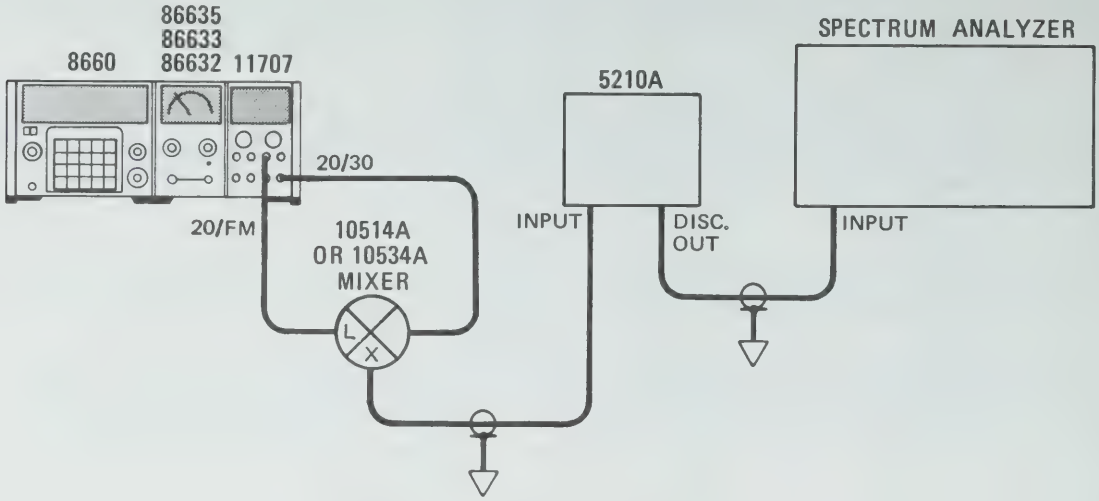


Figure G-2. FM Measurements

Use the following table to determine if the modulation section distortion is within 1%.

Measure the second and third harmonic levels of the 1 kHz signal relative to the fundamental.

If 2nd harmonic is:	then, 3rd harmonic must be at least to meet spec.
< −40 dB	> −49.6 dB
−40.5 dB	> −46.9 dB
−41 dB	> −45.3 dB
−41.5 dB	> −44.3 dB
−42 dB	> −43.6 dB
−42.5 dB	> −43 dB
−43 dB	> −42.2 dB
−44 dB	> −41.7 dB
−45 dB	> −41 dB
−47 dB	> −40.5 dB
−50 dB	> −40.5 dB
> −55 dB	> −40.1 dB

If the harmonics are within the limits above, the modulation section is functioning properly.

NOTE

For FM distortion problems on 8660A or 8660B mainframes with serial prefixes 1343A and below, see Service Notes 8660B-19 or 8660A-21 to check for the presence of 20 MHz on the 100 MHz reference line from A4A4. This signal, if present, can effect the operation of the 11661 YIG loop.

G-12. 20 MHz Signal Not OK. Install modulation section with cover removed or extender cable HP Part No. 11672-60002. Fold back the rear casting and measure the 20 MHz signal with the MODE switch set in FM. The signal should be −4 dBm minimum. If the signal is OK, check the interconnecting cables and connectors between the modulation and RF sections. If the signal is not OK, measure the power supply voltages and if OK, repair the rear panel assembly A7 as required.

G-13. *ϕM Problems.* Set Modulation MODE to ϕM. Set 1000 Hz INTERNAL SOURCE. Modulation Level full scale. Replace RF Section with 11707 Test Plug-in. Set 11707 DC/MOD switch to ϕM and measure output voltage. Should be 1.50 ± 0.075 Vrms. If an 11707 is not available, the ϕM signal may be measured at mainframe J6 pin 59 providing the termination shown in Figure G-3 is used (this termination is built into the 11707).

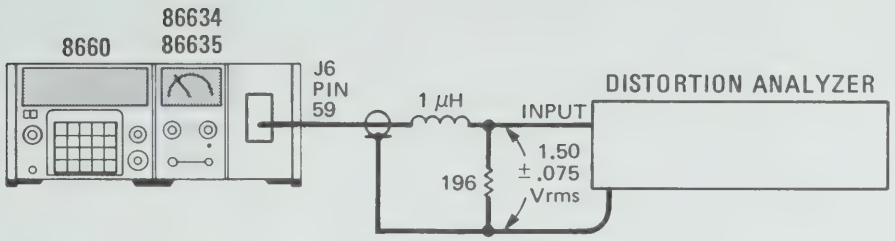


Figure G-3. Phase Modulation Measurements

G-14. If the fundamental signal level is OK, use the 334A distortion analyzer to measure the total harmonic distortion of the ϕM drive signal. It should be less than 1% distortion.

G-15. If the distortion is >1%, troubleshoot ϕM amplifier circuitry in the modulation section. If it is <1%, troubleshoot the Phase Modulator Driver in the RF Section.

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Service needed

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☐ REPAIR ☐ REPAIR & CAL

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Observed symptoms/problems

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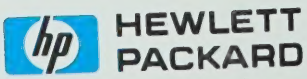

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